EXHIBIT 46

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United States Patent [19]

Hibbard

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[45] Date of Patent: Jan. 17, 1995

[54] **APPARATUS AND METHOD FOR ADAPTIVELY INTERPOLATING A FULL COLOR IMAGE UTILIZING LUMINANCE GRADIENTS**

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[73] Assignee: **Eastman Kodak Company**, Rochester, N.Y.

[21] Appl. No.: **85,520**

[22] Filed: **Jun. 30, 1993**

[51] **Int. Cl.**[6] **H04N 9/07**

[52] **U.S. Cl.** **348/273**; 348/266

[58] **Field of Search** 358/41, 42, 43, 44, 358/163, 213.15, 213.17; H04N 9/07; 348/266, 272, 273

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,630,307	12/1986	Cok	382/25
4,642,678	2/1987	Cok	358/44
5,032,910	10/1989	Cok	358/13
5,040,064	8/1991	Cok	358/163

OTHER PUBLICATIONS

Copending U.S. Patent Application entitled "Apparatus and Method for Adaptively Interpolating a Full Color Image Utilizing Chrominance Gradients", in the name of Claude Laroche and Mark Prescott on even date herewith.

Kodak Professional DCS 200 Digital Camera System, Programmer's Reference Manual, Dec. 1992.

Primary Examiner—James J. Groody
Assistant Examiner—Cheryl Cohen
Attorney, Agent, or Firm—David M. Woods

[57] **ABSTRACT**

Adaptive interpolation is performed by apparatus operating upon a digitized image signal obtained from an image sensor having color photosites that generate a plurality of color values, but only one color per photosite. A digital processor obtains gradient values from the differences between luminance values in vertical and horizontal image directions. The gradient values are compared to a programmable threshold in order to select one of the directions as the preferred orientation for the interpolation of additional luminance values. The interpolation is then performed upon values selected to agree with the preferred orientation.

8 Claims, 3 Drawing Sheets

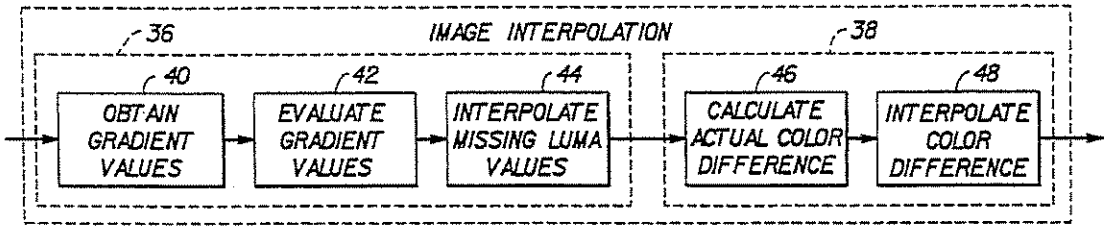


FIG. 1

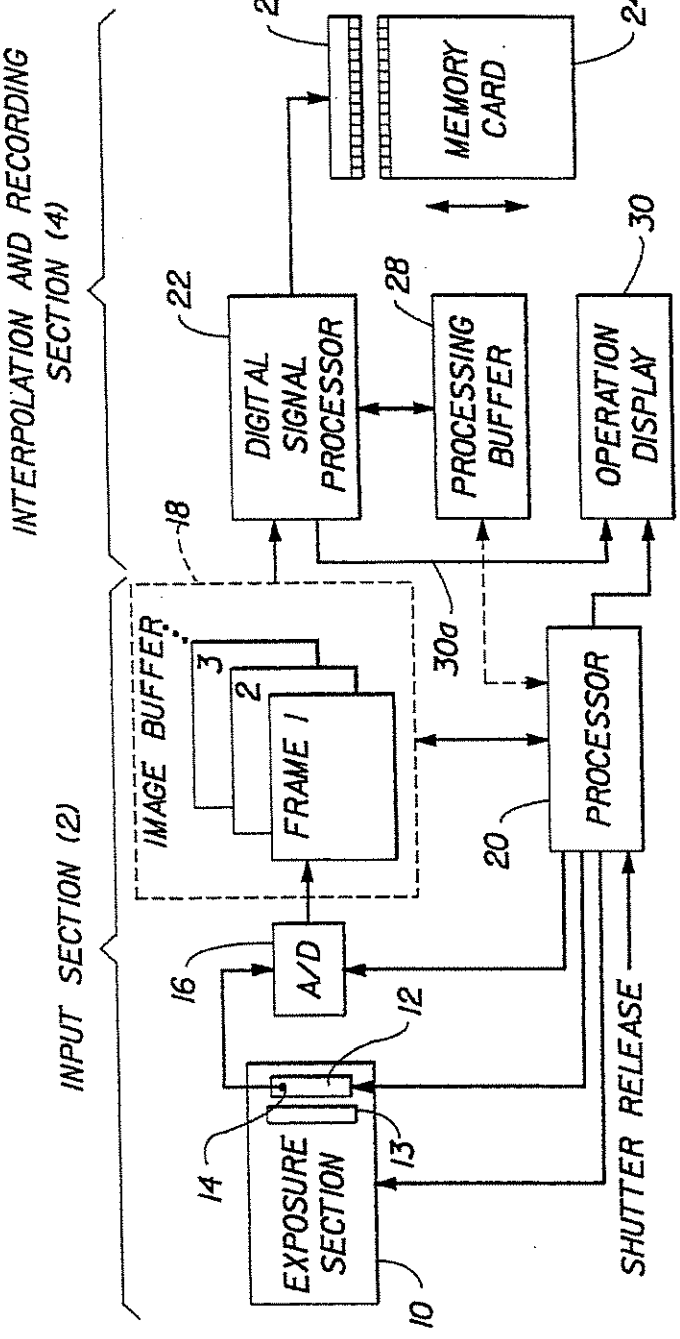
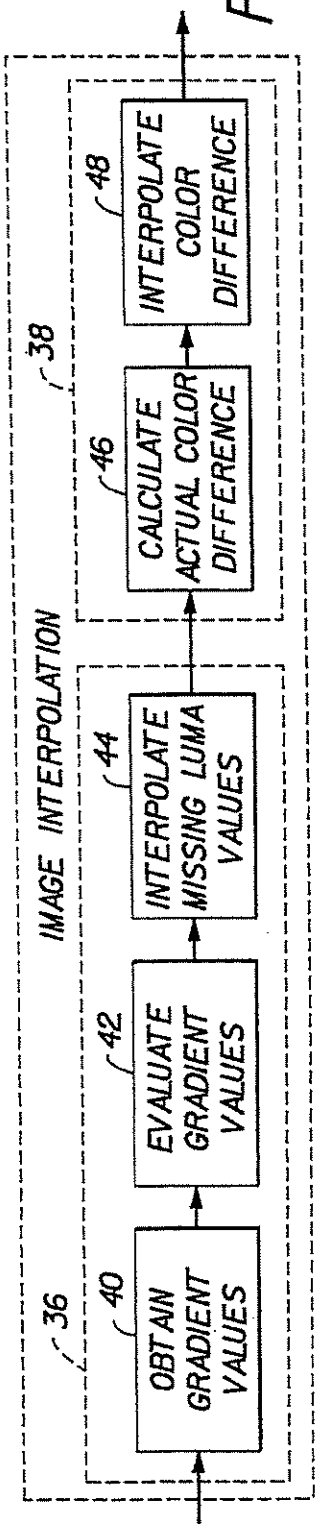


FIG. 2



AXD024510

G	R	G	R	G	R	G
B	G	B	G	B	G	B
G	R	G	R	G	R	G
B	G	B	G	B	G	B

FIG. 3

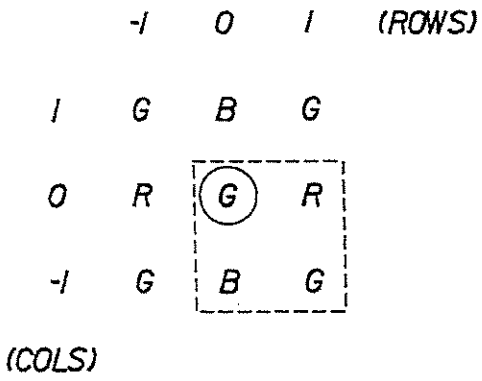


FIG. 4A
(PHASE 00)

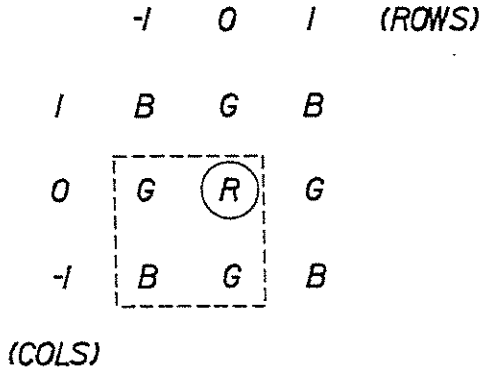


FIG. 4B
(PHASE 01)

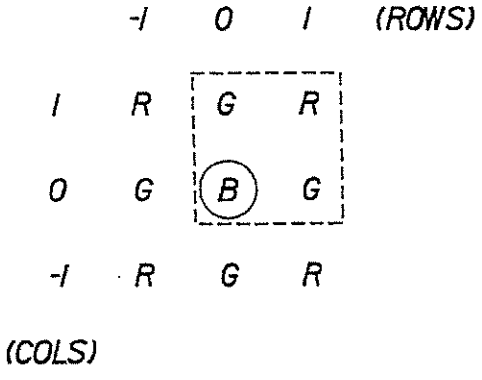


FIG. 4C
(PHASE 10)

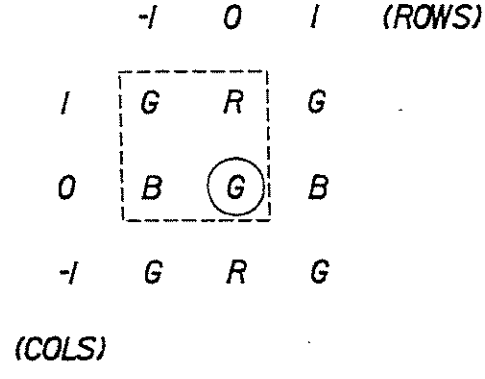


FIG. 4D
(PHASE 11)

AXD024512

APPARATUS AND METHOD FOR ADAPTIVELY INTERPOLATING A FULL COLOR IMAGE UTILIZING LUMINANCE GRADIENTS

FIELD OF INVENTION

This invention pertains to the field of electronic imaging, in particular to the generation of color images.

BACKGROUND OF THE INVENTION

A single-sensor camera detects the spatially varying intensity of light at image locations corresponding to a regular pattern of pixel locations on the sensor. In a color single-sensor camera, a color filter array overlies the sensor such that the sensor detects the intensity of colors at varying pixel locations according to a regular color filter array (CFA) pattern of, generally, three colors. Ordinarily, the CFA is a regular pattern of color filters for detecting only one color at each pixel location. Consequently, a single sensor color camera does not capture original data corresponding to all three colors for each pixel. Instead, it captures one color for each pixel, so that interpolation is required to construct three full color image planes for each image.

A typical camera system generates red, green, and blue colors. A color filter array interpolation algorithm is used to convert the image from a sparsely sampled color image (one color per pixel) to a full red, green, blue (RGB) image (i.e., RGB for each pixel). Most color filter array patterns have a high-frequency signal that is sampled more regularly, and more frequently, in the pattern than the other colors. In an RGB image, this high frequency signal is green; it is also referred to as the luminance signal, which represents the higher frequency detail and the maximum sensitivity of the human eye. Ordinarily, traditional bilinear interpolation is used to generate a full green image plane. For instance, the green data from green pixels on either side of a red or blue pixel (i.e., a "missing green" pixel) are used to interpolate the "missing green" value for the red or blue location. Then, traditional bilinear interpolation of color difference signals, also called chrominance signals, is utilized to interpolate the other colors of the CFA pattern for each pixel. A traditional method of this type is disclosed in U.S. Pat. No. 4,642,678.

A problem with such traditional methods is that they are prone to colored edge artifacts in the image. This problem can be treated through use of more sophisticated interpolation techniques, such as described in U.S. Pat. No. 4,630,307, which uses prior knowledge about features existing in the neighborhood. The image data is utilized to determine the appropriate algorithm, and the missing data is reconstructed using the selected algorithm. For example, in the '307 patent, different interpolation routines are used for edges, stripes, and corners. The particular feature is determined by comparing the pixel data with templates stored in a computer.

As pointed out before, the major shortcoming of the traditional procedures concerns the generation of artifacts at color edges. The sophisticated procedure, exemplified by the '307 patent, can reduce these artifacts, but at considerable cost and complexity in processing capability.

SUMMARY OF THE INVENTION

An object of the present invention is to modify prior, sophisticated algorithms so as to reduce color edge artifacts and to improve image sharpness, without unduly increasing cost and complexity.

A further object of the invention is to perform interpolation in a simplified, adaptive manner in order to reduce color edge artifacts, reduce noise in the image, and to improve image sharpness.

The above-stated objects are realized by apparatus for processing a digitized image signal obtained from an image sensor having color photosites that generate a plurality of color values, but only one color value for each photosite location. Such apparatus includes

a) means for storing the digitized image signal as an image-wise pattern of luminance and chrominance values, wherein some photosite locations lack luminance values; and

b) a processor operative with said storing means for generating a luminance value missing from a photosite location by the interpolation of an additional luminance value for such locations from luminance values at nearby photosite locations. In accordance with the invention the processor includes

a) means for generating gradient values from the differences between luminance values in at least two image directions;

b) means for comparing the gradient values to one or more thresholds;

c) means responsive to the threshold comparison for selecting one of said at least two image directions as a preferred orientation for the interpolation of an additional luminance value; and

d) means for interpolating the additional luminance value from luminance values selected to agree with the preferred orientation.

The principal advantage of the invention is that it can reduce color artifacts without adding undue complexity to the processing.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in relation to the drawings, wherein:

FIG. **1** is a block diagram of an electronic still camera employing interpolation processing according to the invention;

FIG. **2** is a block diagram of the interpolation processing technique used in connection with the invention;

FIG. **3** is a diagram of the Bayer geometry for a color filter array; and

FIGS. **4A–4D** show four phases of the Bayer geometry useful in explaining the interpolation technique.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Since single-sensor electronic cameras employing color filter arrays are well known, the present description will be directed in particular to elements forming part of, or cooperating more directly with, apparatus and method in accordance with the present invention. Elements not specifically shown or described herein may be selected from those known in the art.

Referring initially to FIGS. **1** and **2**, an electronic still camera is divided generally into an input section **2** and an interpolation and recording section **4**. The input section **2** includes an exposures section **10** for directing image light from a subject (not shown) toward an image sensor **12**. Although not shown, the exposure section **10** includes conventional optics for directing the image

light through a diaphragm, which regulates the optical aperture, and a shutter, which regulates exposure time. The sensor **12**, which includes a two-dimensional array of photosites corresponding to picture elements of the image, is a conventional charge-coupled device (CCD) using either well-known interline transfer or frame transfer techniques. The sensor **12** is covered by a color filter array (CFA) **13**, known as the Bayer array, which is described in U.S. Pat. No. 3,971,065 and herewith incorporated by reference. The Bayer geometry is shown in FIG. **3**, wherein each color covers a photosite, or picture element (pixel), of the sensor. In particular, chrominance colors (red and blue) are interspersed among a checkerboard pattern of luminance colors (green). The sensor **12** is exposed to image light so that analog image charge information is generated in respective photosites. The charge information is applied to an output diode **14**, which converts the charge information to analog image signals corresponding to respective picture elements. The analog image signals are applied to an A/D converter **16**, which generates a digital image signal from the analog input signal for each picture element. The digital signals are applied to an image buffer **18**, which may be a random access memory (RAM) with storage capacity for a plurality of still images.

A control processor **20** generally controls the input section **2** of the camera by initiating and controlling exposure (by operation by the diaphragm and shutter (not shown) in the exposure section **10**), by generating the horizontal and vertical clocks needed for driving the sensor **12** and for clocking image information therefrom, and by enabling the A/D converter **16** in conjunction with the image buffer **18** for each signal segment relating to a picture element. (The control processor **20** would ordinarily include a microprocessor coupled with a system timing circuit.) Once a certain number of digital image signals have been accumulated in the image buffer **18**, the stored signals are applied to a digital signal processor **22**, which controls the throughput processing rate for the interpolation and recording section **4** of the camera. The processor **22** applies an interpolation algorithm to the digital image signals, and sends the interpolated signals to a conventional, removable memory card **24** via a connector **26**.

Since the interpolation and related processing ordinarily occurs over several steps, the intermediate products of the processing algorithm are stored in a processing buffer **28**. (The processing buffer **28** may also be configured as part of the memory space of the image buffer **18**.) The number of image signals needed in the image buffer **18** before digital processing can begin depends on the type of processing, that is, for a neighborhood interpolation to begin, a block of signals including at least a portion of the image signals comprising a video frame must be available. Consequently, in most circumstances, the interpolation may commence as soon as the requisite block of picture elements is present in the buffer **18**.

The input section **2** operates at a rate commensurate with normal operation of the camera while interpolation, which may consume more time, can be relatively divorced from the input rate. The exposure section **10** exposes the sensor **12** to image light for a time period dependent upon exposure requirements, for example, a time period between 1/1000 second and several seconds. The image charge is then swept from the photosites in the sensor **12**, converted to a digital format, and written into the image buffer **18** during a standard rate, which may, for example, correspond to a standard video field or frame rate. The repetition rate of the driving signals provided by the control processor **20** to the sensor **12**, the A/D converter **16** and the buffer **18** are accordingly generated to achieve such a transfer. The processing throughput rate of the interpolation and recording section **4** is determined by the speed of the digital signal processor **22**.

One desirable consequence of this architecture is that the processing algorithm employed in the interpolation and recording section may be selected for quality treatment of the image rather than for throughput speed. This, of course, can put a delay between consecutive pictures which may affect the user, depending on the time between photographic events. This is a problem since it is well known and understood in the field of still video recording that a digital still camera should provide a continuous shooting capability for a successive sequence of images. For this reason, the image buffer **18** shown in FIG. **1** provides for storage of a plurality of images, in effect allowing a series of images to "stack up" at video rates. The size of the buffer is established to hold enough consecutive images to cover most picture-taking situations.

An operation display panel **30** is connected to the control processor **20** for displaying information useful in operation of the camera. Such information might include typical photographic data, such as shutter speed, aperture, exposure bias, color balance (auto, tungsten, fluorescent, daylight), field/frame, low battery, low light, exposure modes (aperture preferred, shutter preferred), and so on. Moreover, other information unique to this type of camera is displayed. For instance, the memory card **24** would ordinarily include a directory signifying the beginning and ending of each stored image. This would show on the display **30** as either (or both) the number of images stored or the number of image spaces remaining, or estimated to be remaining.

The digital signal processor **22** interpolates each still video image stored in the image buffer **18** according to the interpolation technique shown in FIG. **2**. The interpolation of missing data values at each pixel location follows the sequence shown in FIG. **2**; that is, first, the high frequency information for the "missing green" pixels (i.e., the red and blue pixel locations) are interpolated to improve the luminance rendition and, secondly, the color difference information is interpolated at the high frequency locations by traditional bilinear methods to generate the other color of the CFA pattern. In the implementation shown in FIG. **2**, an adaptive interpolation technique is used in the luminance section **36** for optimizing the performance of the system for images with horizontal and vertical edges. "Missing green" pixels are adaptively interpolated either horizontally, vertically or two-dimensionally depending upon the gradient established between the green pixel locations in the vertical and horizontal directions around the "missing green" pixel.

The first step is therefore to obtain gradient values, as represented by the block **40**, in at least two image directions, for instance, horizontal and vertical directions. In each direction, the gradients comprise differences between luminance values at spatially-displaced pixel locations. The horizontal and vertical gradients of the luminance (green) pixels are then evaluated relative to a threshold value in an evaluation block **42**, and a pre-

ferred orientation for the interpolation of an additional luminance value is selected from the two directions. The luminance values are selected to agree with the preferred orientation, and the missing location is then averaged in block **44** from the two luminance(green) locations situated along whichever gradient is below the threshold. (Four pixels are averaged when both gradients are less than or greater than the selected threshold level.) Then, the color difference is calculated in a chroma section **38** by subtracting the interpolated green value at each chrominance pixel location (block **46**) from the actual color pixel for that location. Finally, the color difference data for each luminance pixel location is interpolated using two-dimensional bilinear interpolation in the block **48**. The data at this point may be reconstructed into its original components (RGB) or left as color-difference signals for further processing.

In interpolating green data for pixel locations (red and blue) where green data is missing, the image gradients in horizontal and vertical directions are compared to a threshold level, thereby adaptively adjusting the processing to suit the image data. Moreover, the threshold level is itself adjustable to categorize the area of the image being interpolated. In this way, the interpolation may be adjusted to systems having various noise levels and to sensors having different modulation transfer functions.

The four categories of image data determined from these gradient evaluations are:

A. For (Horizontal Gradient>Threshold) and (Vertical Gradient>Threshold), the image areas represent high scene spatial detail. The four pixels are averaged since there is no evident scene structure.

B. For (Horizontal Gradient<=Threshold) and (Vertical Gradient>Threshold), the image areas represent predominately horizontal scene structure. Interpolation is performed by averaging horizontally to follow the scene contours and to minimize error caused by scene edges. This also maximizes image sharpness since scene contour information is not "averaged out" of the image.

C. For (Horizontal Gradient>Threshold) and (Vertical Gradient<=Threshold), the image areas represent predominately vertical scene structure. Interpolation is performed by averaging vertically to follow the scene contours and to minimize error caused by scene edges. This also maximizes image sharpness since scene contour information is not "averaged out" of the image.

D. For (Horizontal Gradient<=Threshold) and (Vertical Gradient<=Threshold), the image areas represent little scene structure. The four pixels are averaged since this reduces the noise level of the interpolated pixel locations. This performs some "noise" reduction in the flat-field areas of the image.

Although not limited to any particular CFA pattern, the interpolation technique has been applied to an RGB Bayer color filter array, as shown in FIG. 3. One characteristic of the Bayer array is that it contains a repetition of RGB in a characteristic Bayer block form, as follows

G R
B G

with two luminances (greens) always on one diagonal, and two chromas (red and blue) on the other diagonal. The object of the interpolation is to obtain all three colors (RGB) for each pixel location.

In FIGS. **4A–4D**, the characteristic Bayer block is shown in four phases (as outlined) with respect to one pixel (circled) that is to be interpolated. Each pixel is identified by its row and column position. In each phase, the notation G(X,Y), R(X,Y) and B(X,Y) are values measured by the image sensor **12** for given horizontal displacements (X) and vertical displacements (Y) from the interpolated (circled) pixel. Adap G(X,Y) is an interpolated green value, using the following algorithm:

For Gdiff-hor=|G(−1,0)−G(1,0)| Gdiff-ver=|G(0,−1)−G(0,1)| Threshold=Predetermined value

If (Gdiff-hor<Threshold) and (Gdiff-ver<Threshold)

Or (Gdiff-hor>Threshold) and (Gdiff-ver>Threshold) Then |Adap G(X,Y)=[G(−1,0)+G(1,0)+G(0,−1)+G(0,1)]/4|

If (Gdiff-hor<Threshold) and (Gdiff-ver>Threshold) Then |Adap G(X,Y)=[G(−1,0)+G(1,0)]/2|

If (Gdiff-hor>Threshold) and (Gdiff-ver<Threshold) Then |Adap G(X,Y)=[G(0,−1)+G(0,1)]/2|

As specifically applied to the four phases of FIGS. 4A–4D, the processing algorithms are as follows.

Phase 00 (FIG. 4A)

G = G(0,0)
B = 0.5 * [B(0,−1) − Adap G(0,−1) + B(0,1) − Adap G (0,1)] + G (0,0)
R = 0.5 * [R(−1,0) − Adap G(−1,0) + R(1,0) − Adap G(1,0)] + G(0,0)

Phase 01 (FIG. 4B)

R = R(0,0)
G = Adap G(0,0)
B = 0.25 * [B(−1,−1) − Adap G(−1,−1) + B(−1,1) − Adap G(−1,1) + B(1,−1) − Adap G(1,−1) + B(1,1) − Adap G(1,1)] + Adap G(0,0)

Phase 10 (FIG. 4C)

B = B(0,0)
G = Adap G(0,0)
R = 0.25 * [R(−1,−1) − Adap G(−1,−1) + R(−1,1) − Adap G(−1,1) + R(1,− 1) − Adap G(1,−1) + R(1,1) − Adap G(1,1)] + Adap G(0,0)

Phase 11 (FIG. 4D)

G = G(0,0)
R = 0.5 * [R(0,− 1) − Adap G(0,−1) + R(0,1) − Adap G(0,1)] + Adap G(0,0)
B = 0.5 * [B(−1,0) − Adap G(−1,0) + B(1,0) −Adap G(1,0)] + Adap G(0,0)

It should be clear from the several phases that green (luminance) is adaptively interpolated for the phases lacking green data (Phases 01 and 10) for the interpolated (circled) pixel. Red or blue (chrominance) is directly available from the sensor for phases 01 and 10. Red and blue (chrominance) is bilinearly interpolated in the other cases by reference to color differences (R−G, B−G) from locations in the neighborhood of the interpolated (circled) pixels. The color differences are then summed with the luminance for the interpolated (circled) pixel to obtain red and blue.

While the interpolation technique of the invention has been described for use in an electronic camera, it may be incorporated as part of other apparatus for processing color data from an image sensor. For instance, the actual data from the image sensor **12** may be down-

loaded directly to the memory card 24, and the interpolation processing may take place subsequently when the card 24 is inserted into a player apparatus. The interpolation technique shown in FIG. 2 will then take place in the player. Such a "player" may in practice be a desktop computer, and the interpolation technique of FIG. 2 is performed by a program in the computer.

The invention has been described in detail with particular reference to a presently preferred embodiment, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

What is claimed is:

1. Apparatus for processing a digitized image signal obtained from an image sensor having color photosites that generate a plurality of color values, but only one color value for each photosite location, said apparatus comprising:

means for storing the digitized image signal as a pattern of luminance and chrominance values, wherein some photosite locations lack luminance values;

a processor operative with said storing means for generating an additional luminance value missing from a photosite location by the interpolation of the additional luminance value for such locations from luminance values at nearby photosite locations, said processor including

means for generating gradient values from the differences between luminance values in at least two image directions;

means for comparing the gradient values to one or more thresholds;

means responsive to the threshold comparison for selecting one of said at least two image directions as a preferred orientation for the interpolation of the additional luminance value; and

means for interpolating the additional luminance value from luminance values selected to agree with the preferred orientation.

2. Apparatus as claimed in claim 1 wherein said one or more thresholds are adjustable.

3. Apparatus as claimed in claim 1 wherein said at least two image directions are horizontal and vertical directions.

4. Apparatus as claimed in claim 1 wherein said pattern of luminance and chrominance comprises chrominance values interspersed in a checkerboard pattern of luminance values.

5. Apparatus as claimed in claim 4 wherein said luminance color is green, and said chrominance colors are red and blue.

6. A method for interpolating missing luminance values from a digitized image signal obtained from a color image sensor having photosites that generate a pattern of actual luminance and chrominance values, one actual value for each photosite location, said method comprising the steps of:

obtaining gradient values from the differences between actual luminance values in vertical and horizontal image directions;

comparing the gradient values to a predetermined threshold;

selecting the image direction, in which the comparing step indicates scene structure, for the interpolation of the missing luminance values; and

interpolating each missing luminance value from actual luminance values at nearby locations corresponding with the selected direction, and thereby with the scene structure.

7. Apparatus as claimed in claim 4 wherein the gradient values are developed from luminance values from photosites immediately adjacent the photosite for which said additional luminance value is interpolated.

8. A method as claimed in claim 6 wherein the gradient values are developed from luminance values from photosites immediately adjacent the photosite for which said additional luminance value is interpolated.

* * * * *

EXHIBIT 47

United States Patent [19]

Vogel et al.

[11] **Patent Number: 4,750,041**

[45] **Date of Patent: Jun. 7, 1988**

[54] **APPARATUS FOR MERGED FIELD OPERATION OF AN IMAGE SENSOR IN A STILL VIDEO CAMERA**

[75] Inventors: **Richard M. Vogel**, Henrietta; **Mitchell J. Milton**, Webster; **Thomas C. Nutting**, Fairport, all of N.Y.

[73] Assignee: **Eastman Kodak Company**, Rochester, N.Y.

[21] Appl. No.: **96,814**

[22] Filed: **Sep. 10, 1987**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 898,968, Aug. 21, 1986, abandoned.

[30] **Foreign Application Priority Data**

Aug. 10, 1987 [WO] PCT Int'l Appl. PCT/US87/01901

[51] **Int. Cl.**[4] **H04N 3/15**

[52] **U.S. Cl.** **358/213.22**; 358/909; 358/213.13

[58] **Field of Search** 358/213.13, 213.19, 358/213.22, 213.28, 213.29, 909

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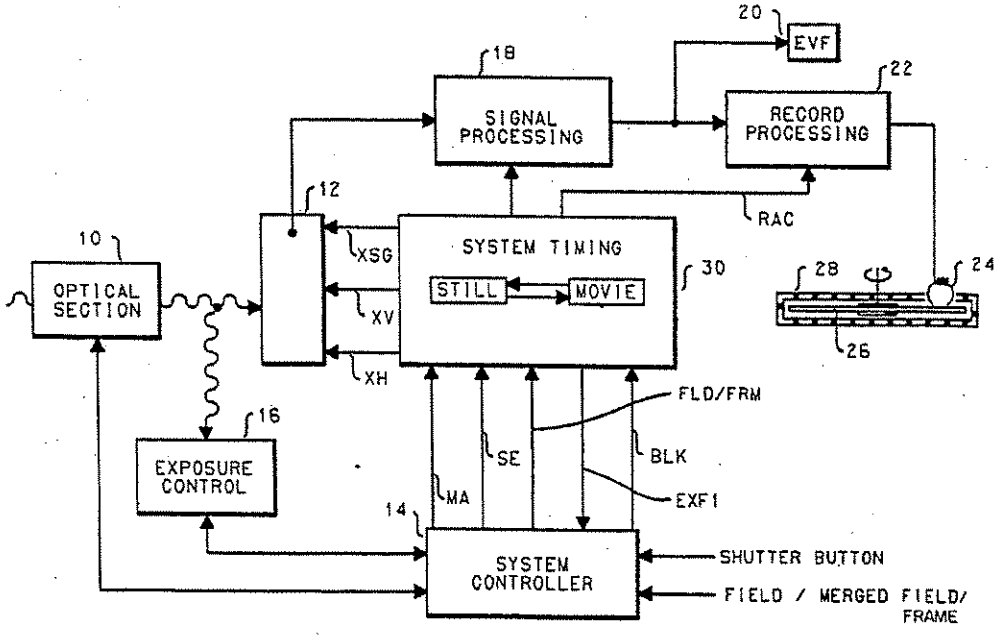
Primary Examiner—Jin F. Ng
Assistant Examiner—Stephen Brinich
Attorney, Agent, or Firm—David M. Woods

[57] **ABSTRACT**

A driving circuit (**30**) generates multi-phase signals for operating the vertical charge-coupled registers (**V1**, **V2** . . .) of an interline-transfer image sensor (**12**). Though having full-frame still capability, the sensor (**12**) is included in a still video camera for single-field recording. After a still exposure is completed, the phase signals (**XV1** . . . **XV4**) applied to the vertical registers generate an array of charge wells in the registers alongside the photoelectric elements (**P1**, **P2**) corresponding to each field. The image charges residing in these elements transfer to the registers as separate fields, where they are merged as one field in order to increase the photosensitivity for a single-field still recording. Such increased photosensitivity is translated into increased photographic range by controlling the exposure of the sensor (**12**) to accord with the increased image charge by, for example, reducing the exposure time provided by the sensor or the optical aperture presented to the image sensor. In this manner, the "speed" of the sensor is increased for merged field operation.

7 Claims, 9 Drawing Sheets



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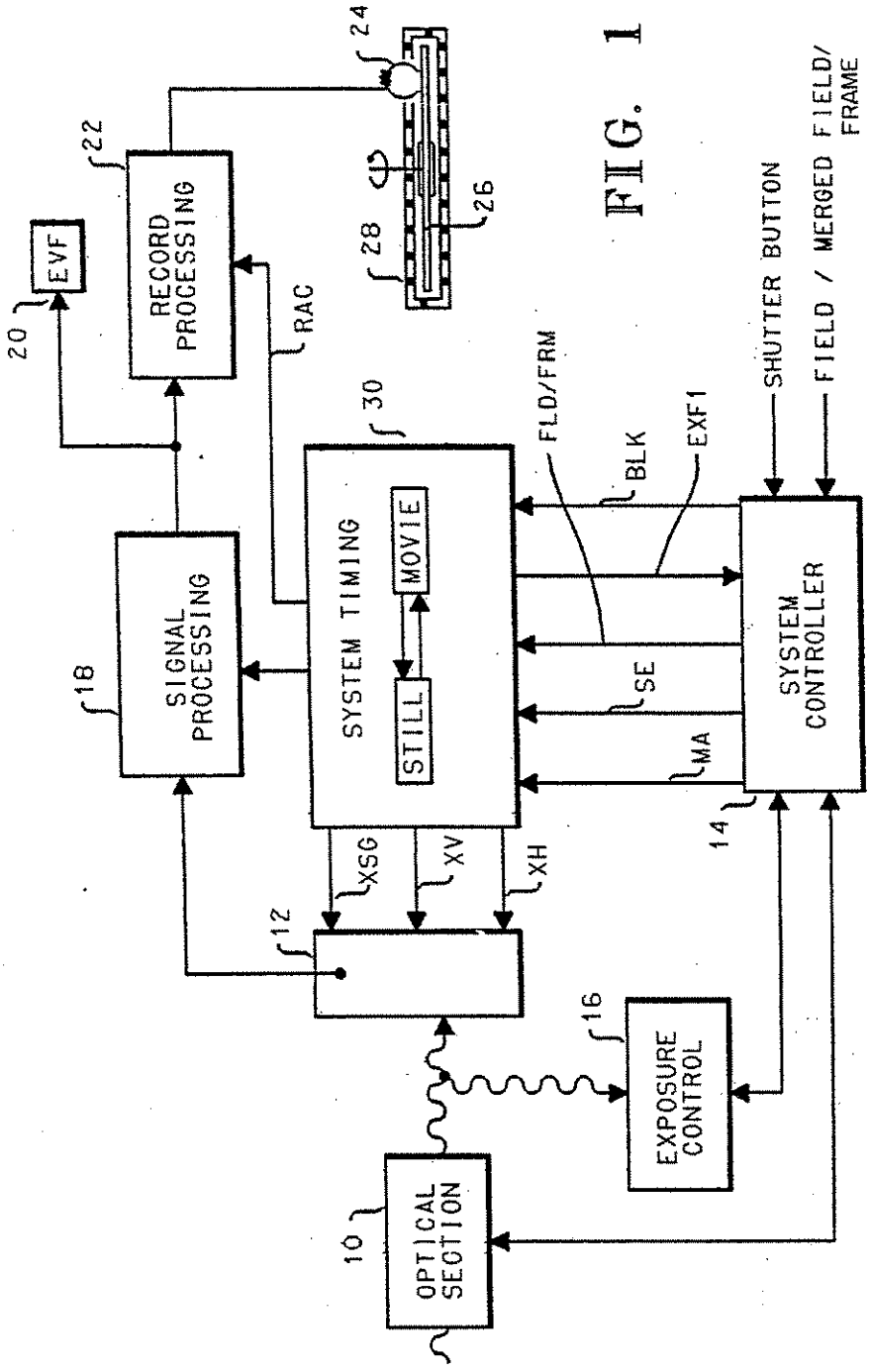

24
22
RECORD PROCESSING
EVF
20
RAC
26
28
30
SYSTEM TIMING
MOVIE
STILL
FLD/FRM
BLK
EXF1
SHUTTER BUTTON
FIELD / MERGED FIELD/ FRAME
SYSTEM CONTROLLER
SE
MA
14
18
SIGNAL PROCESSING
XSG
XV
XH
12
16
EXPOSURE CONTROL
10
OPTICAL SECTION

FIG. 1

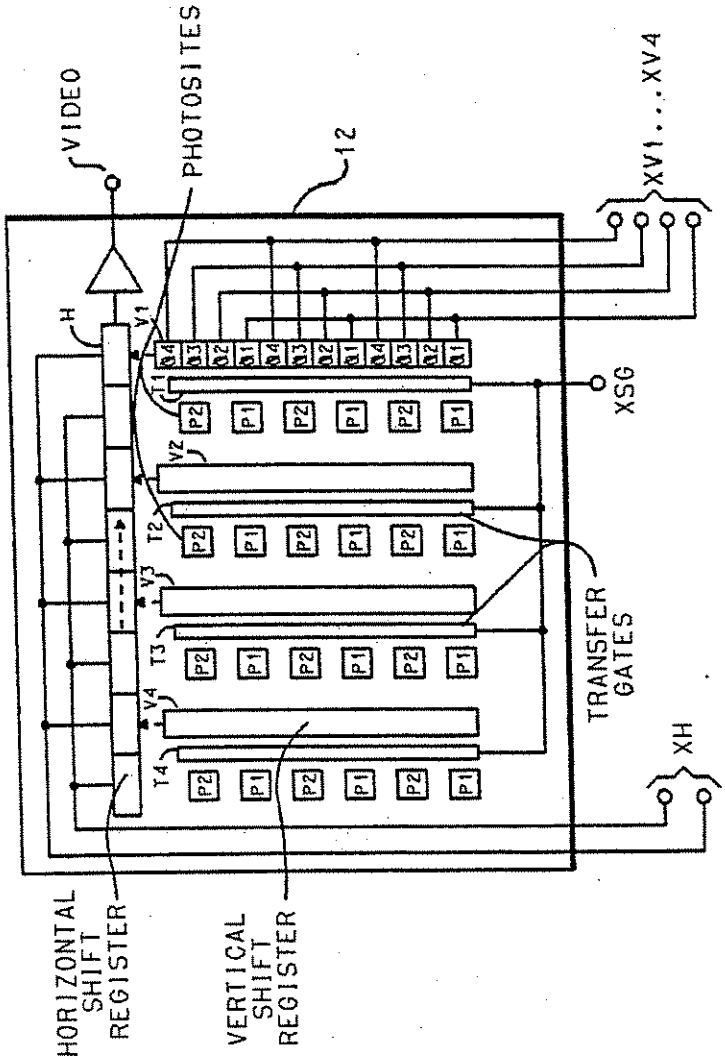

VIDEO
PHOTOSITES
12
XV1...XV4
H
V1
T1
XSG
V2
T2
V3
T3
V4
T4
TRANSFER GATES
XH
HORIZONTAL SHIFT REGISTER
VERTICAL SHIFT REGISTER

FIG. 2

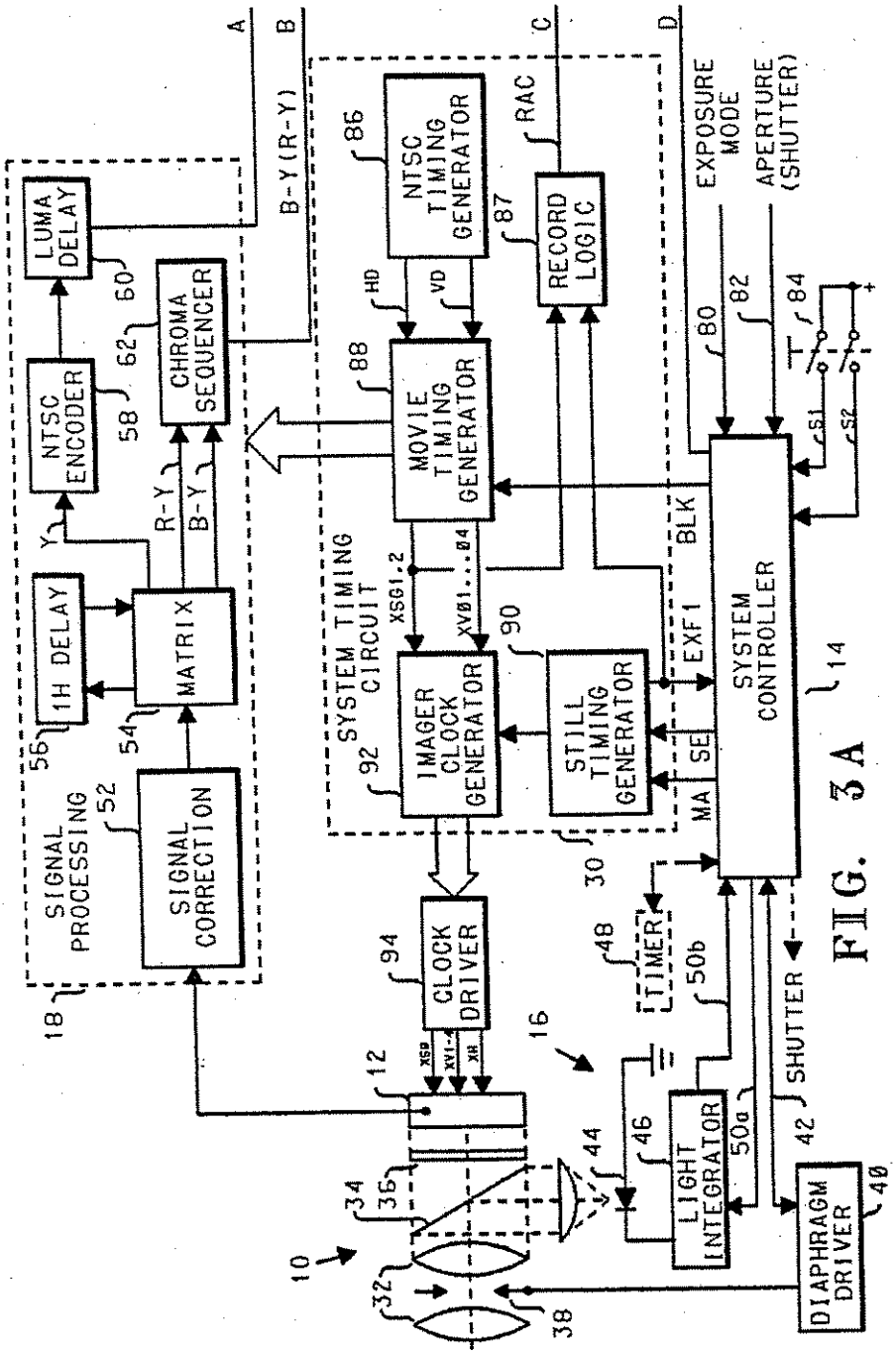

A
B
C
D
B-Y(R-Y)
LUMA DELAY
60
CHROMA SEQUENCER
62
NTSC ENCODER
58
1H DELAY
56
MATRIX
54
SIGNAL PROCESSING
52
SIGNAL CORRECTION
18
Y
R-Y
B-Y
NTSC TIMING GENERATOR
86
HD
VD
RAC
RECORD LOGIC
87
MOVIE TIMING GENERATOR
88
SYSTEM TIMING CIRCUIT
XSG1,2
XV01...04
IMAGER CLOCK GENERATOR
92
STILL TIMING GENERATOR
90
CLOCK DRIVER
94
XSG
XV1-4
XIR
12
16
EXPOSURE MODE
APERTURE (SHUTTER)
80
82
84
S1
S2
BLK
EXF1
SE
MA
SYSTEM CONTROLLER
14
30
TIMER
48
50b
SHUTTER
LIGHT INTEGRATOR
46
50a
42
DIAPHRAGM DRIVER
40
44
34
36
32
38
10

FIG. 3A

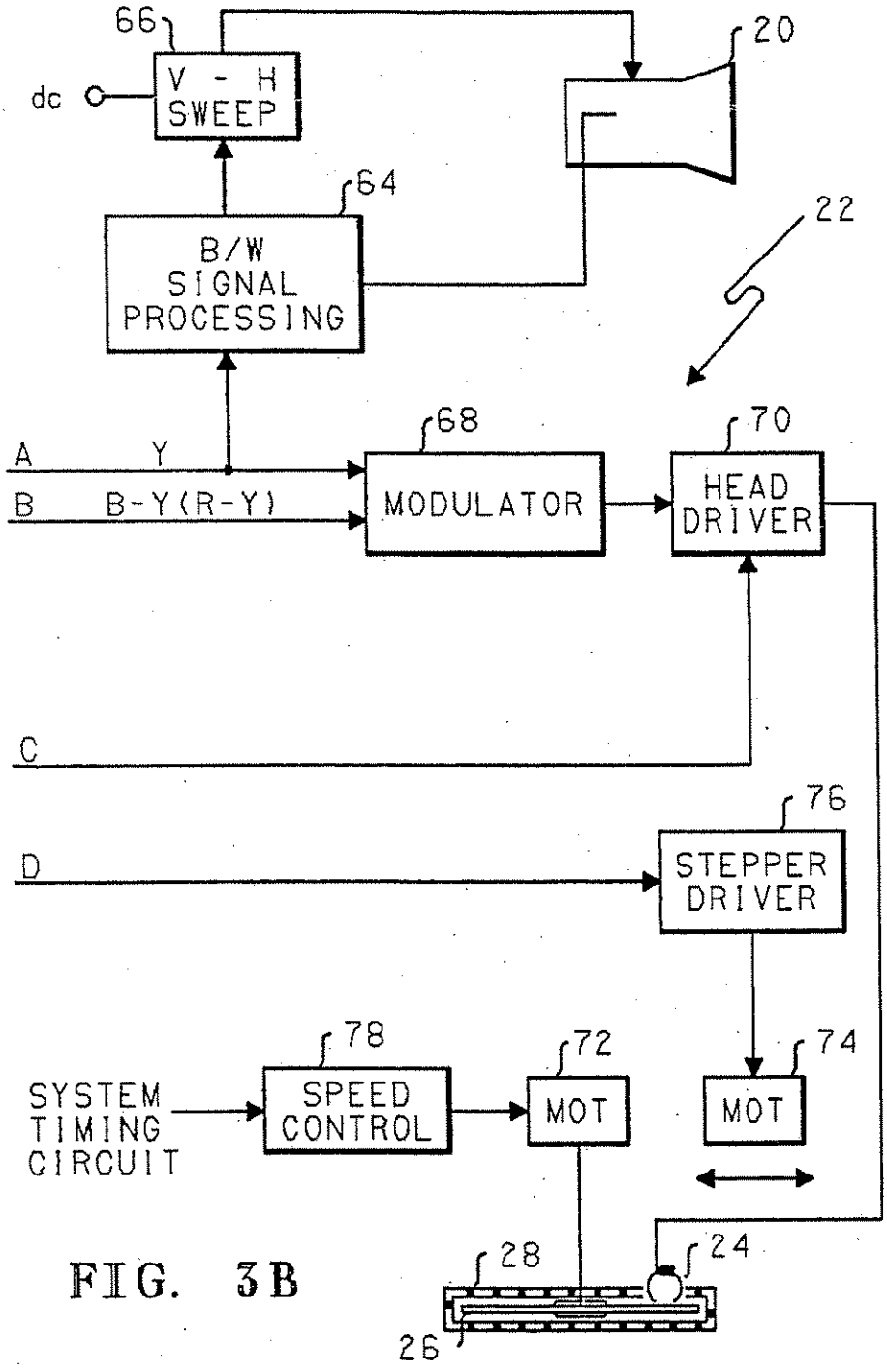

66
V - H SWEEP
dc
20
64
B/W SIGNAL PROCESSING
22
68
70
A Y
B B-Y(R-Y)
MODULATOR
HEAD DRIVER
C
76
D
STEPPER DRIVER
78
72
74
SYSTEM TIMING CIRCUIT
SPEED CONTROL
MOT
MOT
28
24
26

FIG. 3B

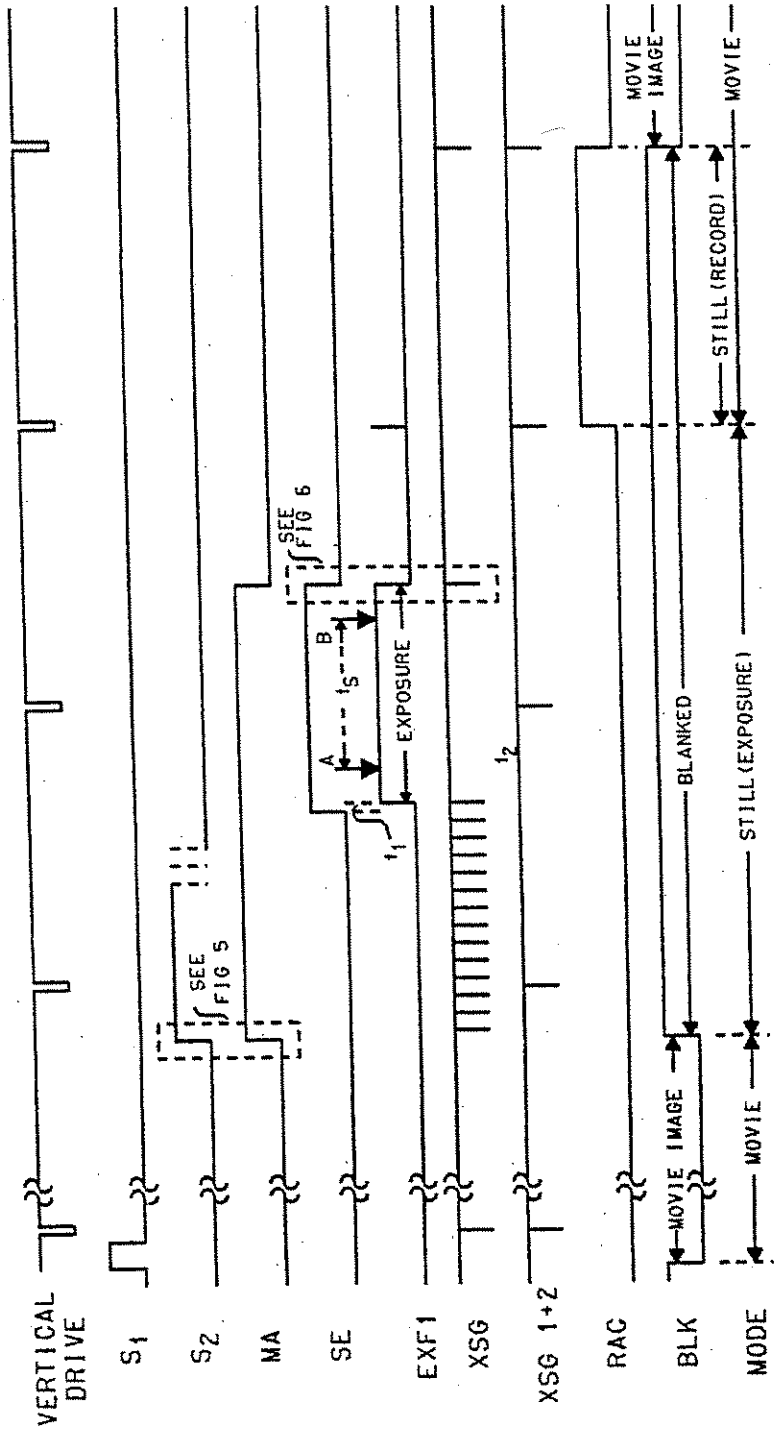

VERTICAL DRIVE
S1
S2
MA
SE
EXF1
XSG
XSG 1+2
RAG
BLK
MODE
SEE FIG 5
SEE FIG 6
A
B
EXPOSURE
MOVIE IMAGE
BLANKED
STILL (EXPOSURE)
STILL (RECORD)
MOVIE

FIG. 4

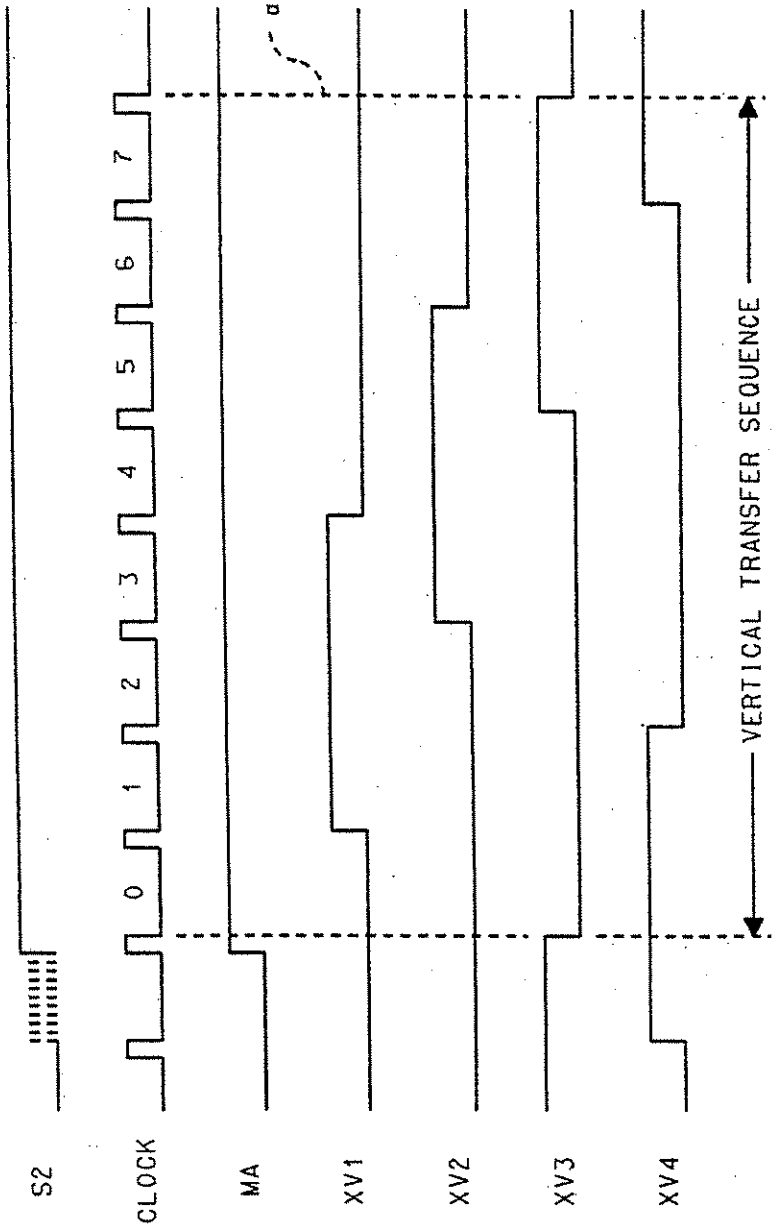

S2
CLOCK
MA
XV1
XV2
XV3
XV4
0
1
2
3
4
5
6
7
a
VERTICAL TRANSFER SEQUENCE

FIG. 5

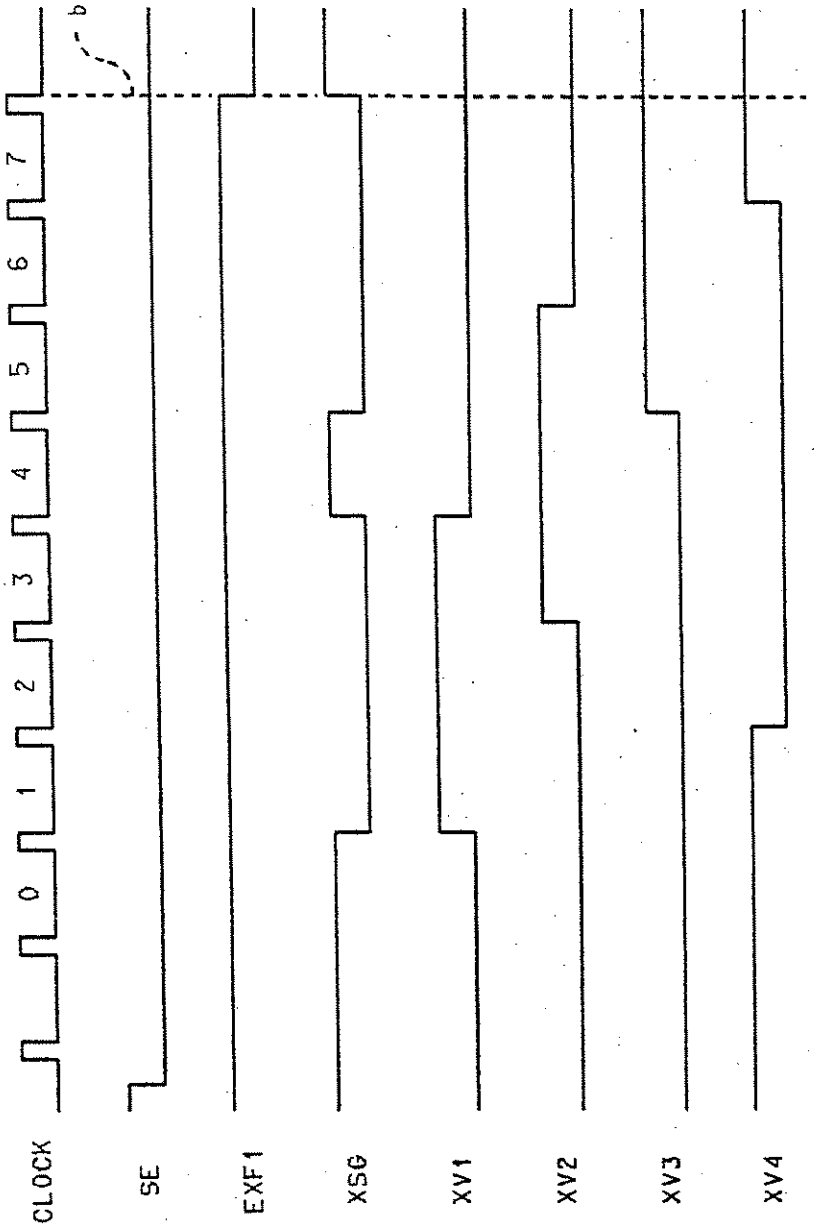


FIG. 6

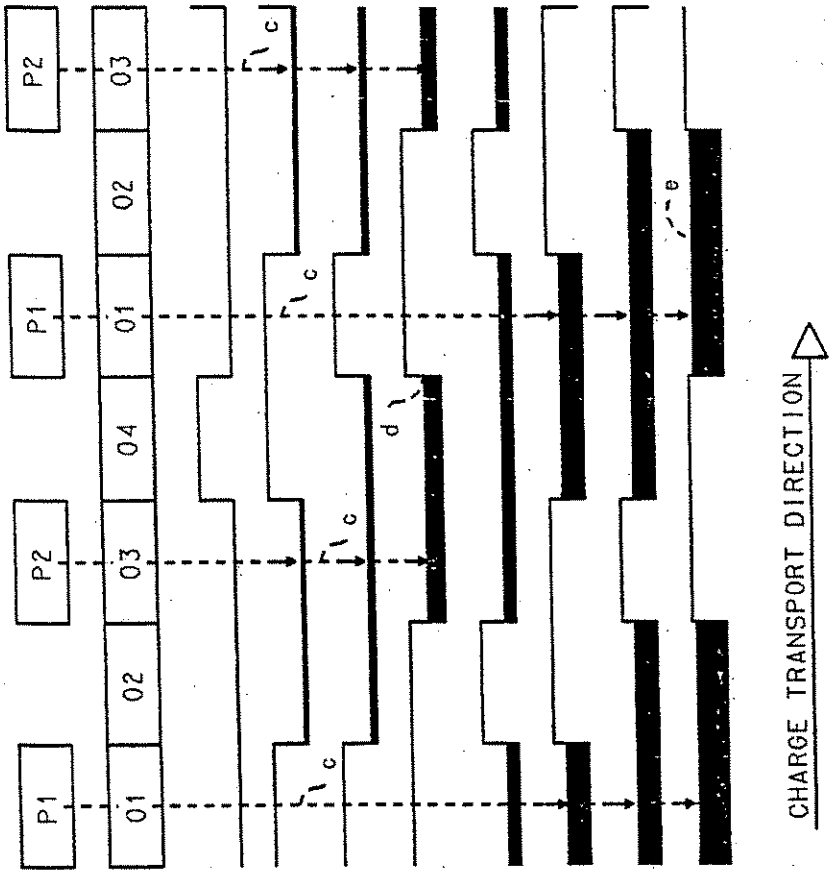
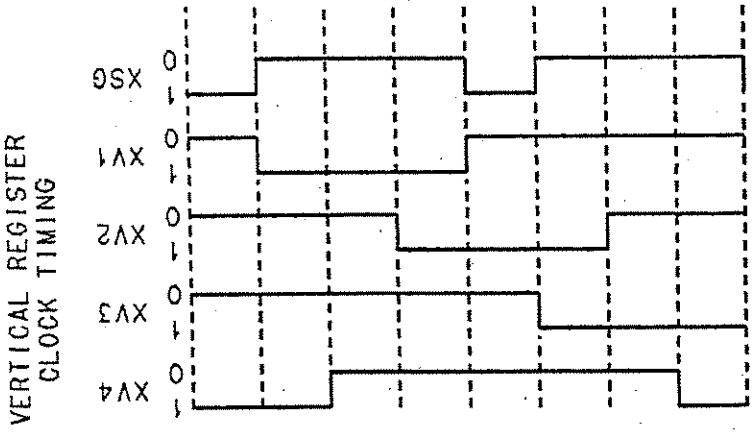

P2
P1
P2
P1
O3
O2
O1
O4
O3
O2
O1
c
d
e
CHARGE TRANSPORT DIRECTION

FIG. 7


VERTICAL REGISTER CLOCK TIMING
XSG
XV1
XV2
XV3
XV4
0
1

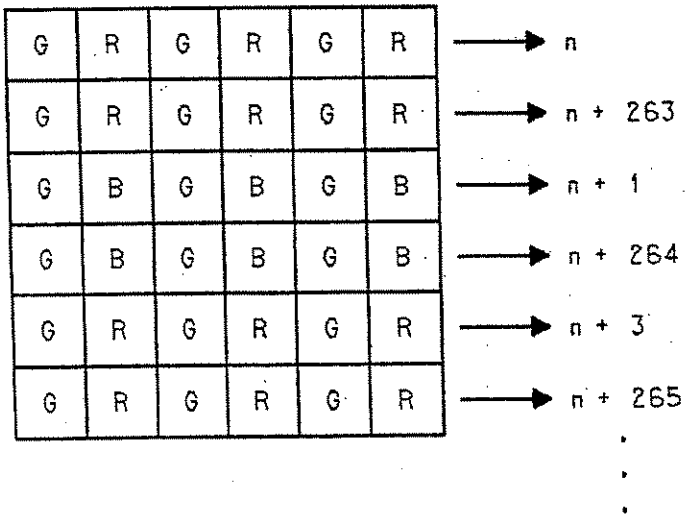

G R G R G R
G R G R G R
G B G B G B
G B G B G B
G R G R G R
G R G R G R
n
n + 263
n + 1
n + 264
n + 3
n + 265

FIG. 8

APPARATUS FOR MERGED FIELD OPERATION OF AN IMAGE SENSOR IN A STILL VIDEO CAMERA

CROSS-REFERENCE TO RELATED APPLICATIONS

This is a continuation-in-part of application Ser. No. 898,968, filed Aug. 21, 1986, now abandoned.

This application is related to (1) copending patent application Ser. No. 882,121, entitled "Asynchronous Still Timing for a Video Camera Producing Movie or Still Images", filed on July 3, 1986, in the name of R. Vogel and (2) copending patent application Ser. No. 880,461, entitled "Exposure Control Apparatus For a Still Video Camera Having an Electronic Viewfinder", filed on June 30, 1986 in the name of T. Nutting and R. Shroyer.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of still video imaging, and especially to the operation of an image sensor in a camera capable of producing a single-field recording.

2. Description Relative to the Prior Art

A new video recording format has been introduced in which a small flexible magnetic disk is used to store up to 50 still video pictures. This format provides the option of storing a full frame (two circular tracks per picture) for 25 pictures, or a single field (one circular track per picture) for 50 pictures. Though single field recording inevitably limits playback resolution compared to full-frame recording, a satisfactory "full-frame" result can be played back by interpolating a second field from successive lines of the recorded (first) field. U.S. Pat. No. 4,470,076 illustrates such interpolation with a still image obtained from a limited-resolution, single-field image sensor. The principal attractiveness of single field recording is the higher picture density obtained on the recorded disk. Nonetheless, frame recording provides an inherently better result. A versatile video camera would therefore offer the user both capabilities: frame and field recording.

Frame recording requires that color information regarding both fields be simultaneously generated within an image sensor capable of separately resolving, and outputting, each field. Without simultaneously-generated fields, any movement between fields would provide an unsightly image. Since the aforementioned still format provides line sequential color, each line of the image sensor must separately provide the necessary primary color signals (R, G or B) for generating a line sequential color difference (R−Y or B−Y). A typical sensor of this type employs an interline-transfer technique. In such a sensor, photo-generated charges stored in the odd horizontal lines are read out for the odd video field, while the other line charges are read out for the even field. Such sensor operation can be compared with a video (movie) operating method called "frame integration", in which photo-generated electrons in each photoelectric element are accumulated for one television frame time, i.e., 1/30 second in the NTSC system. In a still video camera, however, the photo-generated electrons in each photoelectric element are accumulated for a variable period dependent upon the required still exposure.

Significantly, line charges must be maintained distinct so that one field is unaffected by charges from the other field. In this way, the fields are temporarily separable though they have been concurrently integrated. (Another movie mode, referred to as "field integration", requires the addition of line charges in two adjacent lines in order to generate the primary color signals. Field integration is unsuitable for full-frame still imaging because it depends on a successive generation of two fields to provide a frame. In other words, each field "uses up" all the charge accumulated by the sensor and the sensor must be re-exposed for the second field. For a discussion of both field and frame integration, see "Field Integration Mode CCD Color Television Camera Using a Frequency Interleaving Method", by Koshinori Takizawa et al, *IEEE Trans. on Consumer Electronics*, Vol. CE-29, No. 3, August 1983, pp. 358–364.)

In a still video camera having a full-frame interline-transfer image sensor with concurrent field integration, the provision for single field recording uses only half of the photoelectric elements of the sensor. Drawing an analogy to conventional photographic film, the effective "resolution" of the sensor is reduced accordingly. With film, however, resolution can be traded for "film speed", that is, lowering resolution ordinarily leads to an increase in photosensitivity. This does not happen with an electronic sensor operating in a field mode because the light sensitivity of the sensor is dependent upon half the photoelectric elements in half the area of the sensor. No benefit in "speed" is obtained.

U.S. Pat. No. 4,603,354 discloses an electronic camera having an image sensor operable in either a still frame mode or a still field mode, in both cases using each field. Odd and even fields are produced and read out separately in the frame mode. The field mode, on the other hand, provides a "merged" output by the addition of the information charges of both fields. For the merged field, the information charge put out by the image sensor is double that put out for each field in the frame mode—each image location has twice as much charge. As a result, since the information charge in the frame and merged field modes is different, either attenuating or amplifying means are provided for adjusting the level of the signal from the image sensor. In this way, the two modes provide equal output. This level adjustment, however, provides two unattractive alternatives: either increase the gain of the frame signal, thereby adding noise to the supposedly "high quality" signal, or decrease the gain of the merged field signal, thereby reducing effective photosensitivity in the potentially "high speed" signal.

Disclosure of Invention

Instead of trying to extend photographic range in merged field operation by modifying the level of the signal from the image sensor, it turns out that modifying the exposure of the image sensor provides greater range without having to trade noise for sensitivity. A conventional interline-transfer sensor can thus be adapted for either full frame or merged field use in a still camera without requiring level changes in the signal output from the sensor. In merged field operation, a field is output from the sensor at, for instance, double the output level compared to full-frame operation under the same exposure. This happens because all the image charge is collected in one field. Knowing this, the light exposure of the sensor is adjusted in the merged field operational mode to take advantage of the additional

"sensitivity". For instance, either the optical aperture or the exposure time of the sensor is reduced, which has the effect of extending low light scene capability for the same output as in full-frame operation. Then the picture signal is recorded. Considering that the field is replicated, or interpolated, during payback (to obtain the second field), the effect is to double the "speed" of the sensor compared to full-frame operation.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described with reference to the drawings, in which:

FIG. 1 is a block diagram of a still video camera incorporating merged field operation according to the invention;

FIG. 2 is an illustration of a conventional interline-transfer image sensor used in the camera of FIG. 1;

FIG. 3(A and B) is a rendition of the block diagram of FIG. 1 in further detail;

FIG. 4 is a timing diagram describing signal conditions during the operation of the camera shown by FIG. 3;

FIG. 5 is a detailed expansion of the beginning of still mode timing as shown by FIG. 4;

FIG. 6 is a detailed expansion of the end of the still exposure period as shown by FIG. 4;

FIG. 7 is a composite diagram showing some of the timing waveforms of the image sensor and the corresponding charge transfers that produce a merged field according to the invention; and

FIG. 8 is a diagram of a section of a known color mosaic filter used in connection with an imager sensor operated according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Because video cameras and video cameras employing interline-transfer image sensors are well known, the present description will be directed in particular to elements forming part of, or cooperating more directly with, apparatus in accordance with the present invention. Elements not specifically shown or described herein may be selected from those known in the art.

Referring initially to FIG. 1, the pertinent sections of a still video camera are shown for purposes of describing the invention: An optical section 10 directs image light to an image sensor 12, which in its preferred form is a conventional solid-state, interline-transfer image sensor. The basic elements of a conventional interline-transfer image sensor are shown schematically in an abbreviated form in FIG. 2. Briefly, the light gathered by the optical section 10 causes charge to collect in an array of photosites (photoelectric elements) disposed in rows and columns on a semiconductor substrate. A plurality of photosites P1 are disposed in rows and columns for generating a pattern of electrical signals corresponding to a first video field; likewise, a second plurality of photosites P2 generate signals corresponding to a second video field. A group of imager driving signals (XSG, XV and XH) determine the operation of the sensor—in the case of a charge-coupled device, certain of these signals (XV and XH) prescribe a phase-related control of charge movement, hence the term phasing signals.

When the transfer gate signal XSG is low, the image charges that have collected in a selected plurality (field) of photosites transfer through a set of transfer gates $T_1 \ldots T_4$ to a corresponding set of vertical charge-coupled (CCD) shift registers $V_1 \ldots V_4$. Each vertical shift register is divided into a repetitive series of phase sections $\phi 1 \ldots \phi 4$. A set of vertical phasing signals XV1 . . . XV4 are applied to respective phase sections $\phi 1 \ldots \phi 4$ to transfer the charges to a horizontal CCD shift register H, from which they are transferred off the image sensor by a horizontal phasing signal XH. Vertical and horizontal transfers are accomplished by biasing the registers with the respective phasing signals to form an array of independent potential wells, which are then shifted by varying the bias levels of the phasing signals in tandem. The selection of a particular field is obtained by biasing the vertical registers V1 . . . V4 such that a potential well appears at a phase section $\phi 1$ (field 1) or $\phi 3$ (field 2) when the transfer gates T1 . . . T4 are opened.

Referring back to FIG. 1, a system controller 14, preferably a microprocessor, controls the general operation of the camera, including the optical section 10 and an exposure control circuit 16. A video signal generated by the image sensor 12 is converted into a line sequential color signal by a signal processing section 18. A monochrome rendition of the signal is displayed upon an electronic viewfinder 20 and, at the appropriate time, the color signal is prepared for recording in a record processing section 22. The recording signal is applied to a recording head 24 and recorded upon a magnetic disk 26. The disk 26 is mounted for rotation within a cartridge housing 28, which has an opening that allows the recording head 24 to contact the disk 26 for recording a plurality of concentric tracks (which correspond to a plurality of images). A timing circuit 30 synchronizes the signal processing section 18, the record processing signal 22, and the viewfinder 20, with the image sensor 12. In particular, the timing circuit 30 produces the transfer gate signal XSG, and the phasing signals XV1 . . . XV4 and XH.

A number of additional signals are shown in FIG. 1, as follows: A moving aperture signal MA (from the controller 14 to the timing circuit 30) signifies that a shutter button has been pressed for a still exposure and that the optical aperture presented to incoming light is being adjusted by the optical section 10. A start exposure signal SE (from the controller 14 to the timing circuit 30) follows the signal MA and signifies that the aperture is correctly established and a still exposure can begin. An expose field signal EXF1 (from the timing circuit 30 to the controller 14) then indicates that the still exposure indeed has begun. A blanking signal BLK (from the controller 14 to the timing circuit 30) controls the blanking of the electronic viewfinder 20. The recording period is regulated by a record activate signal RAC (from the timing circuit 30 to the record processing section 22). Each of these signals will be further described in connection with FIGS. 3 and 4.

Merged field operation of the still video camera of FIG. 1 involves, as will be described, the summing of image charges residing in the first plurality of photosites P1 with the image charges residing in the second plurality of photosites P2. Since both fields of image charge are initially present on the image sensor shown by FIG. 2, the camera can be operated in either a conventional single-field or dual-field (full frame) mode, as well as the merged field mode that is the subject of this invention. A special input line is provided to the system controller 14 for selecting the mode of operation. The specification of frame or field recording is signified by the state of a signal FLD/FRM applied to the timing circuit 30.

While not shown in detail in FIG. 1, full frame operation involves either moving the head 24 from one track to the next for recording both fields, or the provision of a dual head structure for recording both fields sequentially without head movement. FIG. 3, which shows the presently preferred embodiment, is devoted to merged field operation and, as such, may either represent a camera that provides only merged field recording or that part of a full-featured camera devoted to merged field recording. In any case, single-field (unmerged) operation and dual-field (full frame) operation are conventional techniques that will not be further addressed. The mode selection and FLD/FRM signals are thus not shown as separate inputs to the controller 14 and timing circuit 30 in FIG. 3.

Referring to FIG. 3A, the optical section 10 includes a lens system 32 for directing image light from an object (not shown) to the image sensor 12 through a partially transmissive mirror 34 and a color filter 36. The color mosaic structure of the filter 36 may be any kind that affords completely separate fields . . . that is, each field has all the color information necessary for its own set of color primaries. A section of a suitable, and presently preferred, color mosaic is shown in FIG. 8, together with the lines represented by each row. (In movie operation, such a color mosaic is typical of a "frame integration mode" color filter.) Returning to FIG. 3A, a diaphragm 38 regulates the optical aperture (through which image light passes) by a linkage with a diaphragm driver 40. The system controller 14 and the driver 40 communicate with one another on a line 42 when the aperture is to be changed. The optical section 10 also interacts with the exposure control circuit 16, which receives a sample of image light diverted by the mirror 34. The exposure control circuit 16, which employs an integration cycle in its exposure determination process, includes a photodiode 44 and a light integrating circuit 46 that cooperate with a timing procedure (shown by a broken-line box 48) in the system controller 14 to arrive at a brightness value of the incoming image light. The appropriate aperture setting of the diaphragm 38 for either the full-frame or merged field mode is determined from the brightness value. The light integrator 46 is enabled by the system controller 14 on a line 50*a*; when the integration cycle is complete, a signal is returned to the controller 14 on a line 50*b*. A description of this integration cycle can be found in further detail in copending cross-referenced application (2), Ser. No. 880,461.

The video signal generated by the image sensor 12 (by application of the aforementioned signals XSG, XV1 . . . XV4 and XH) is maintained nominally the same (for the same image light) regardless of operational mode by either reducing the aperture setting of the diaphragm 38 or by shortening the exposure time of the image sensor 12 during merged field operation. Whichever mode is in use, the video signal is applied to a signal correction circuit 52, which performs a sample and hold operation and applies gain, white balance and gamma corrections to the signal. The color signal is applied to a matrix 54, which, in combination with a set 56 of 1H delay lines, produces a luminance (Y) signal, and a pair of color difference signals (B−Y, R−Y). The luminance signal is applied to a NTSC encoder 58 and a luma delay stage 60, the latter mainly to account for subsequent color delays in the modulation process. Meanwhile the color difference signals are put in line sequence by a chroma sequencer 62. The luminance signal is tapped at this point (see FIG. 3B) and directed through a monochrome (B/W) signal processing circuit 64 to the electronic viewfinder 20 (which is a conventional monochrome display). The viewfinder display is controlled by conventional vertical and horizontal sweep circuits 66.

The luminance signal and the color difference signals are input to a modulator 68, which provides a selected preemphasis to the input signals and frequency modulates a suitable set of carriers with the preemphasized signals. When permitted by the condition of the record activate signal RAC from the system timing circuit 30, the modulated signal is amplified by a head driver circuit 70 and applied to the recording head 24. The recording portion of the camera includes a disk drive motor 72 for rotating the magnetic disk 26 adjacent the recording head 24. The head 24 is moved by a stepper motor 74 that is connected to a stepper driver circuit 76 controlled from the system controller 14. The disk drive motor 72 is operated at a constant speed by a speed control circuit 78 coupled to the timing circuit 30.

The system timing circuit 30 and the system controller 14 are mutually adapted for two modes of operation: a movie mode for previewing the actual scene and a still mode for recording a still rendition of the scene. In the movie mode, the exposure time is fixed and the aperture is set to a value determined by the exposure control circuit 16 and the system controller 14. In the still mode, on the other hand, both exposure time and aperture may be varied. One of several conventional exposure modes is selected by designating a unique input to the system controller 14 on a line 80 for the type of mode: for example, aperture-preferred, shutter-preferred, manual, and one or more conventional program modes for emphasizing action photos, for emphasizing depth-of-field, for compromising somewhere between the two preceding modes, and so on. Depending on the exposure mode in use, the exposure time and/or aperture value are manually entered to the system controller 14 on line(s) 82. The movie mode is initiated by partially depressing a two-position shutter button 84 to its first position, thereby setting a signal S_1 high. The still mode is subsequently selected when the shutter button 84 is fully depressed to its second position and an exposure release signal S_2 is set high.

The system control circuit 30 has a free-running circuit component in the form of a NTSC timing generator 86 and a movie timing generator 88, and an intermittently-operated component in the form of a still timing generator 90. The NTSC generator 86 provides a horizontal drive signal HD and a vertical drive signal VD according to NTSC standards. The movie timing generator 88 keys upon the drive signals from the NTSC timing generator 86 and generates a set of transfer gate signals XSG1 and XSG2 for the respective fields of a television frame and a set of four vertical register phasing signals XVϕ1 . . . XVϕ4 for operating the vertical registers of the image sensor according to NTSC timing. The movie timing generator 88 also provides the timing for the signal processing circuit 18, including sample and hold pulses for the signal correction section 52, clamping levels, and so on.

An imager clock generator 92 receives input signals from either the movie timing generator 88 or the still timing generator 90 and applies its output to a clock driver 94, which provides the phasing signals XSG, XV1 . . . XV4 and XH to the image sensor 12. The clock generator 92 serves, in the movie mode, as a conduit for

the vertical phasing signals XVϕ1 . . . XVϕ4 by transferring them directly to the clock driver 94 (where they become the signals XV1 . . . XV4) and, in the still mode, as a generator of the still timing that defines the still exposure sequence. The field transfer gate signals XSG1 and XSG2 are combined in an OR function by the imager clock generator 92 and, in the movie mode, applied to the clock driver 94 as the transfer gate signal XSG seen in connection with FIG. 2. In the still mode, the XSG signal is independently generated in a preliminary sequence to clear the image sensor 12 of extraneous charge and then to define the still exposure period. Though the XSG signal is shown in FIGS. 1, 2, 3A and subsequent Figures as being separately applied to the transfer gates of the image sensor 12, the XSG signal may instead be carried on the vertical phasing signals that drive the vertical registers, thus dispensing with a separate transfer gate. In the preferred embodiment the XSG signal is presented as a higher than usual bias level on one of the vertical phasing signals (XV1 or XV3) at the moment a transfer is called for; the result . . . the transfer of image charge to the vertical registers . . . is the same for either technique. The timing interrelationship of the still mode and the movie mode is shown in greater detail in the cross-referenced application (1), Ser. No. 882,121.

Referring to FIG. 4 in connection with FIGS. 3A and 3B, when the movie mode is initiated by setting the signal S_1 high, the blanking signal BLK from the system controller 14 to the movie timing generator 88 is set low. The movie timing generator 88 accordingly permits the signal processing circuit 18 to pass a video signal to the viewfinder 20. In the movie mode, the timing circuit 30 produces the vertical transfer gate signal XSG for opening the transfer gates of the image sensor according to the vertical drive frequency. Vertical register phasing signals XV1 . . . XV4 and horizontal register phasing signals XH (not shown in FIG. 4) remove the video signal from the image sensor within each field period, applying it to the signal processing section 18 to generate a conventional monochrome video movie display in the viewfinder 20.

The vertical drive signal shown in FIG. 4 determines the video rate for the movie mode of operation. The still mode of operation can be seen from the subsequent waveforms as an interruption of the movie video rate; in particular, both a preliminary sequence of aperture adjustment/sensor clearing and the actual still exposure can be commenced without regard to the vertical drive signal. The still mode is instead initiated in relation to the clock period governing the phase signals XV1 . . . XV4. This clock signal is seen in FIG. 5 as a separate signal that determines the edge transitions of the phasing signals XV1 . . . XV4. The vertical transfer sequence (the time for a potential well to move through the four phase sections ϕ1 . . . ϕ4 of a vertical register) is thus related to a sequence of clock periods. The signal MA, which begins the still mode sequence, is only recognized on the next transition of the clock signal after the still release S2 has been triggered.

Referring again to FIG. 4, with the onset of the signal MA, the signal BLK is set high and the movie timing generator 88 accordingly directs the signal processing circuit 18 to clamp its output signal to a black level. This effectively blanks the viewfinder 20. The system controller 14 issues signals on the line 42 to move the diaphragm to its still aperture value, which was predetermined by operation of the exposure control circuit 16. In the meantime the still timing generator 90 has interrupted the imager clock generator 92 and has initiated a rapid-fire sequence of XSG pulses to the transfer gates of the image sensor 12 to clear the photosites of extraneous unwanted charge. From there the charge is cleared by rapid operation of the vertical and horizontal registers. In this connection, the vertical phasing signals XV1 . . . XV4 shown by FIG. 5 begin a rapid sequence in which each full clearing sequence lasts 1 millisecond. When the aperture is set, a start exposure signal SE is sent to the timing circuit 30 to indicate that an exposure should commence.

Depending on when the signal XSG is last pulsed low during the repetitive fast clearing sequence, a short time interval t_1 elapses before the next clearing sequence is completed following receipt of the signal SE. This time ranges from one clock cycle to a full clearing sequence (1 millisecond). The time interval t_1 terminates with the system timing circuit 30 momentarily dropping the gate signal XSG low one more time to open the image sensor transfer gates. As soon as the transfer gates are closed (XSG is high), the image sensor photosites (both P1 and P2) immediately begin to collect charge from the incident image light and the still exposure period begins. Simultaneously, the timing circuit 30 notifies the system controller 14 with the expose field signal EXF1 that the still exposure has begun. Since there is non-image charge residing in the vertical registers, the phasing signals XV1 . . . XV4 are sequenced one more time (at the fast rate) until the vertical registers are fully cleared. The states of the phasing signals XV1 . . . XV4 then remain in the conditions shown to the right of the broken line (a) of FIG. 5.

During the pre-exposure clearing sequence the signal on the line 50*a* is set low so that the exposure circuit 16 does not operate. At the instant the expose field signal EXF1 goes high, the signal on the line 50*a* likewise goes high, thereby beginning the still exposure control integration cycle in synchronism with the still image exposure cycle. When the still exposure cycle is completed, the signal on the line 50*b* changes state, thus notifying the system controller 14 that the exposure should end. The system controller 14 then notifies the timing circuit 30 that the exposure should end by driving the start exposure signal SE low. (The signal MA is also brought low at this time.)

The transfer gate signal XSG (whether alone or carried by a vertical phasing signal) regulates the transfer of integrated image charge from the photosites to the vertical registers. Since the vertical registers in a conventional interline-transfer device are light-protected by an opaque coating, the image charge is light-protected once it is transferred and the still exposure is terminated. As shown by FIG. 6, the transfer of the image charge into the vertical registers occurs in relation to a transfer sequence of the phasing signals XV1 . . . XV4 (which have been static since the last field of extraneous charge was dumped after the still exposure was started). When the transfer gate signal XSG is pulsed low in conjunction with the low state of the phasing signal XV1 (which is applied to the phase section ϕ1) or XV3 (applied to the phase section ϕ3) the charge residing in the photosites P1 or P2 are transferred into the vertical registers V1 . . . V4. According to the diagram of FIG. 6, this is done first in connection with the charges in the photosites P2. The tandem pulsations of the phasing signals XV1 . . . XV4 then move the trapped charge into the phase sections ϕ1. The gate

signal XSG is again pulsed low, but now in conjunction with the low state of the phasing signal XV1, and the trapped charge is joined by the charge from the plurality of photosites P1. In this manner the two charge patterns are merged to form a combined field, thereby utilizing the full photosensitivity of the image sensor for one field. Since the charge residing in the photosites P1 can be transferred within a very short time after the transfer of charge residing in the photosites P2 (for example, within 30 microseconds), the additional exposure effect upon the later-transferred field is minimal.

The merging of the charges in the two fields is further shown by the combined timing and transport diagram of FIG. 7. The vertical phasing signals XV1 . . . XV4 and the transfer gate signal XSG are shown along the left edge. Field one and field two photosites (P1 and P2) are shown alongside the respective phase sections of a portion of the vertical register V1. The diagrams below the vertical register phase sections $\phi 1 \ldots \phi 4$ indicate the status of each of the register phases at each instant of the phasing signal waveforms (time proceeds vertically according to the broken lines c). A low phase level indicates a potential well—which is capable of holding charge—and a high phase level indicates a barrier—which keeps the wells separate. Charge is transferred during the time signified by the solid arrow heads on the broken lines c. For instance, a charge well is shown partially filled at d with image charge from a photosite P2. The same well is moved alongside the next adjacent photosite P1 and shown filled at e with image charge from both photosites P2 and P1.

After the two video fields are transferred, the expose field signal EXF1 drops low, indicating to the system controller 14 that the exposure is over. The vertical phasing signals XV1 . . . XV4 remain static (as shown to the right of the broken line b in FIG. 6) until the next occurrence of the XSG1 or XSG2 pulse, thus temporarily trapping the merged image charge in place on the image sensor. For this pulse (XSG1 or XSG2) the transfer gate signal XSG is inhibited since the meaningful image charge in the vertical registers must not be contaminated by residual charge that has accumulated in the photosites since the exposure ended. The transfer of control from the still mode to the movie mode takes place at this time and is shown in more detail in the cross-referenced application (1), Ser. No. 882,121. The vertical transfer clock signals $XV\phi 1 \ldots XV\phi 4$ have been temporarily interrupted by the imager clock generator 92, which substituted the timing instructions received from the still timing generator 90. When the signal XSG1 (or XSG2) is first pulsed low by the movie timing generator 88 after the signal SE has dropped low, the transfer of control is obtained, i.e., the vertical clock signals XV1 . . . XV4 are resynchronized to the clock signals $XV\phi 1 \ldots XV\phi 4$ from the movie timing generator 88.

Since the signal processing section 18 is driven by the movie timing generator 88 in either mode, the video information is clocked off the image sensor 12 and processed into a video signal by the circuits making up the section 18. Meanwhile, the concurrence of a XSG1 (or XSG2) pulse and an EXF1 pulse activates a record logic section 87 in the timing circuit 30. The record activate signal RAC is thus set high, which activates the head driver 70, and the still video signal is recorded on the magnetic disk 26. At the occurrence of the next vertical drive interval the transfer gate signal XSG resumes its movie mode of operation and a movie image is displayed on the viewfinder 20, i.e., the signal BLK is set low.

The disclosure thus far has been of an "electronically-shuttered" camera, i.e., a camera without a mechanical shutter. If a mechanical shutter is provided, it would preferably be closed at some point after initiation of the still mode and then opened during the still exposure period (when the signal EXF1 is set high). For instance, referring to the waveform for the signal EXF1 in FIG. 4, the mechanical shutter (not shown separately) would be opened during a period t_s, which is shown to extend in time from an arrow A to an arrow B comprising a portion of the high cycle of the signal EXF1. The exposure control circuit 16 would be accordingly keyed to the period t_s so as to properly determine the exposure. Using a mechanical shutter means that the light-protected vertical registers on the image sensor 12 would not have to be used to protect the image charge. A full-frame exposure could therefore be made and, while the shutter is closed, each field could be separately clocked off the image sensor 12 (frame operation) or both fields could be merged in accordance with the invention (field operation).

The foregoing disclosure describes a still video camera that achieves the greater picture density (50 pictures per magnetic disk) associated with single field recordings without wasting half of the photoelectric charge generated for full-frame image sensing. Merging fields has the effect of concentrating all the image charge in one field, thereby increasing, even doubling, the apparent "speed" of the sensor. Ordinarily, for unchanged exposure of the sensor, merging fields has the effect of increasing, even doubling, the nominal field sequential output of the sensor. If, according to the invention, the amount of light received by the image sensor is reduced when fields are merged, the output of the sensor is maintained nominally uniform (i.e., for the same external light level) whether in the full-frame or merged field mode. This enables lower-light photography for given aperture/shutter conditions or, alternatively, less demanding aperture/shutter conditions for the same light level. For instance, the light received by the image sensor 12 during merged field operation is reduced by closing down the aperture or by shortening the shutter speed (for example, by halving one or the other). In effect, therefore, the "speed" of the sensor is increased for merged field operation because the same signal level is obtained for less sensor exposure, i.e., for a lower image light level upon the sensor. Moreover, by utilizing the vertical registers of an interline transfer register according to the invention, merged field operation is accomplished without affecting full resolution, full frame operation . . . that is, operation wherein each field of the frame is a distinct and complete entity.

The invention has been described in detail with particular reference to a presently preferred embodiment, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention. For example, the camera has been especially set up to operate according to NTSC television standards, but it is clear that, with a suitable image sensor and readily implemented changes in the timing circuits, PAL or SECAM standards could be accommodated as well.

What is claimed is:

1. An electronic still camera capable of either frame or merged field modes of operation, said camera having an optical section for controlling image light directed

toward an image sensor that is capable of producing an output signal corresponding to separate fields, and means for operating the sensor to produce the fields separately (frame operation) or in summed combination (merged field operation), said camera comprising:

means for selecting either frame or merged field operation;

means for adjusting the amount of image light received by the sensor according to the selected operational mode; and

means responsive to said selected operational mode for recording a still video picture either as separate fields or as a single merged field.

2. A camera as claimed in claim 1 in which said optical section includes a shutter and said means for adjusting the amount of image light adjusts the exposure time provided by the shutter.

3. A camera as claimed in claim 1 in which said optical section includes a diaphragm and said means for adjusting the amount of image light adjusts the optical aperture provided by the diaphragm.

4. A camera as claimed in claim 1 in which the image sensor is operated such that its effective exposure interval may be varied and in which said means for adjusting the amount of image light adjusts said effective exposure interval provided by operation of the image sensor.

5. A camera as claimed in claim 1 in which said means for adjusting the amount of image light adjusts said image light received by the sensor so that said output signal thereof is nominally uniform for the same image light regardless of the operational mode selected.

6. A camera as claimed in claim 1 in which said means for adjusting the amount of image light includes means for determining the illumination level of the image light directed toward the sensor and means for determining an exposure time and an aperture from said illumination level.

7. A camera as claimed in claim 1 in which said adjustment of the image light is made for merged field operation.

* * * * *

EXHIBIT 48

United States Patent [19]

Sasson et al.

[11] **Patent Number: 5,016,107**

[45] **Date of Patent: May 14, 1991**

[54] **ELECTRONIC STILL CAMERA UTILIZING IMAGE COMPRESSION AND DIGITAL STORAGE**

[75] Inventors: **Steven J. Sasson**, Hilton; **Robert G. Hills**, Spencerport, both of N.Y.

[73] Assignee: **Eastman Kodak Company**, Rochester, N.Y.

[21] Appl. No.: **349,566**

[22] Filed: **May 9, 1989**

[51] Int. Cl.[5] **H04N 5/225**; H04N 5/30

[52] U.S. Cl. **358/209**; 358/909; 358/906; 358/961.3

[58] Field of Search 358/479, 906, 909, 261.3, 358/427, 229, 335, 209; 360/32, 35.1

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Hashiguchi, Sumihisa, "Possibilities of the Digital Electronic Still Camera", Shashin Kogaku, Feb. 1988, pp. 110–111.

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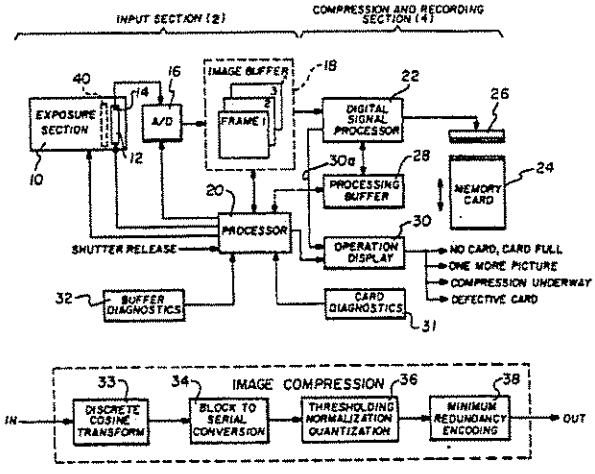
Primary Examiner—James J. Groody
Assistant Examiner—Kim Yen Vu
Attorney, Agent, or Firm—David M. Woods

[57] **ABSTRACT**

An electronic still camera employs digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable static random access memory card. An image sensor is exposed to image light and the resultant analog image information is converted to digital image signals. A control processor controls the exposure section and the A/D converter, delivering digital signals to a multi-image buffer at a rate commensurate with normal operation of the camera. A digital processor operates on the stored digital signals, transforming blocks of the digital signals and encoding the signals into a compressed stream of processed image signals, which are downloaded to the memory card. The digital processor operates at a throughput rate different than the input rate for better image capture and optimum utilization of the camera.

18 Claims, 5 Drawing Sheets



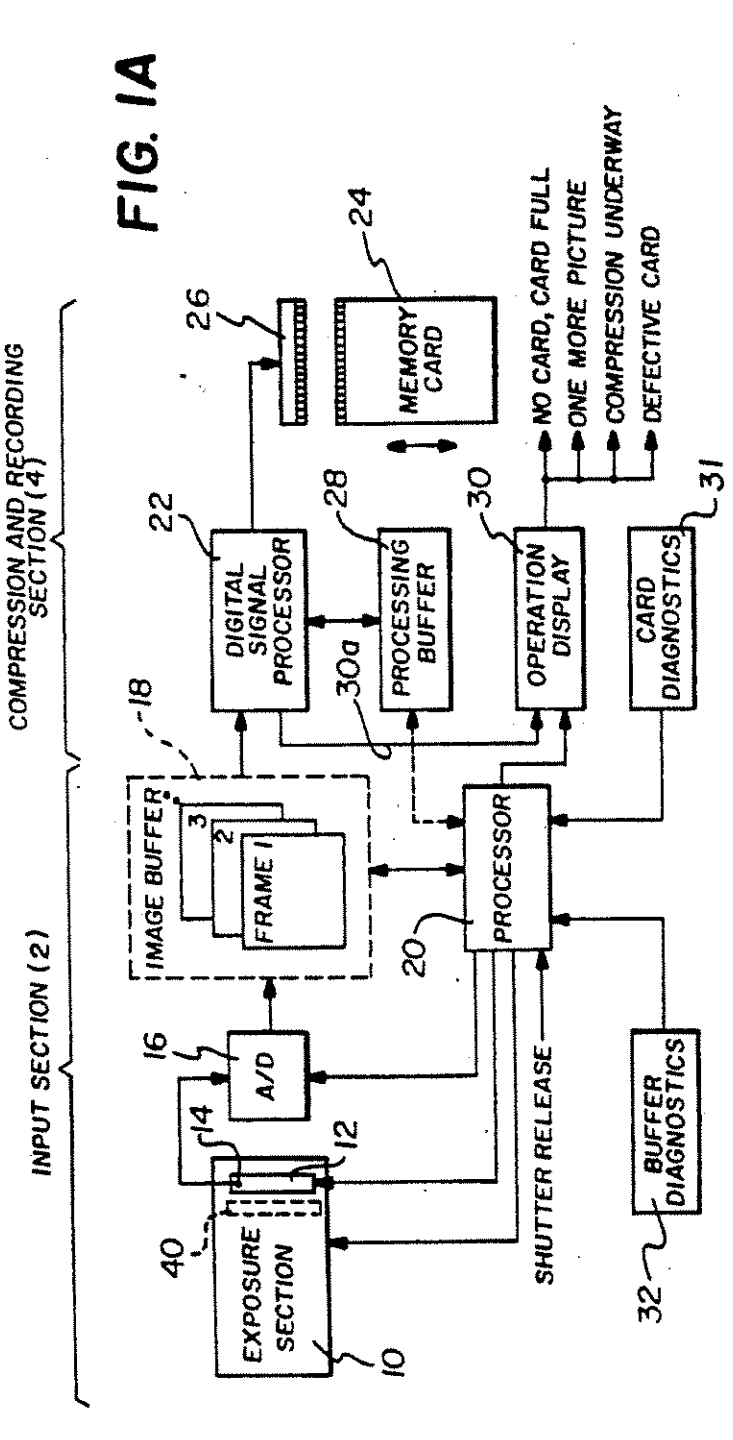


FIG. 1A
COMPRESSION AND RECORDING SECTION (4)
INPUT SECTION (2)
IMAGE BUFFER
FRAME 1
2
3
18
A/D
16
14
12
EXPOSURE SECTION
10
40
DIGITAL SIGNAL PROCESSOR
22
PROCESSING BUFFER
28
30a
PROCESSOR
20
SHUTTER RELEASE
OPERATION DISPLAY
30
CARD DIAGNOSTICS
31
BUFFER DIAGNOSTICS
32
26
MEMORY CARD
24
NO CARD, CARD FULL
ONE MORE PICTURE
COMPRESSION UNDERWAY
DEFECTIVE CARD

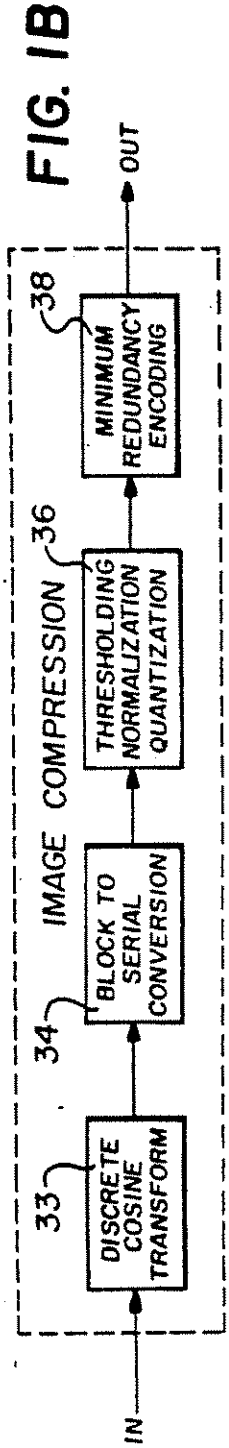


FIG. 1B
IMAGE COMPRESSION
36
38
MINIMUM REDUNDANCY ENCODING
THRESHOLDING NORMALIZATION QUANTIZATION
BLOCK TO SERIAL CONVERSION
34
DISCRETE COSINE TRANSFORM
33
IN
OUT

AX203263

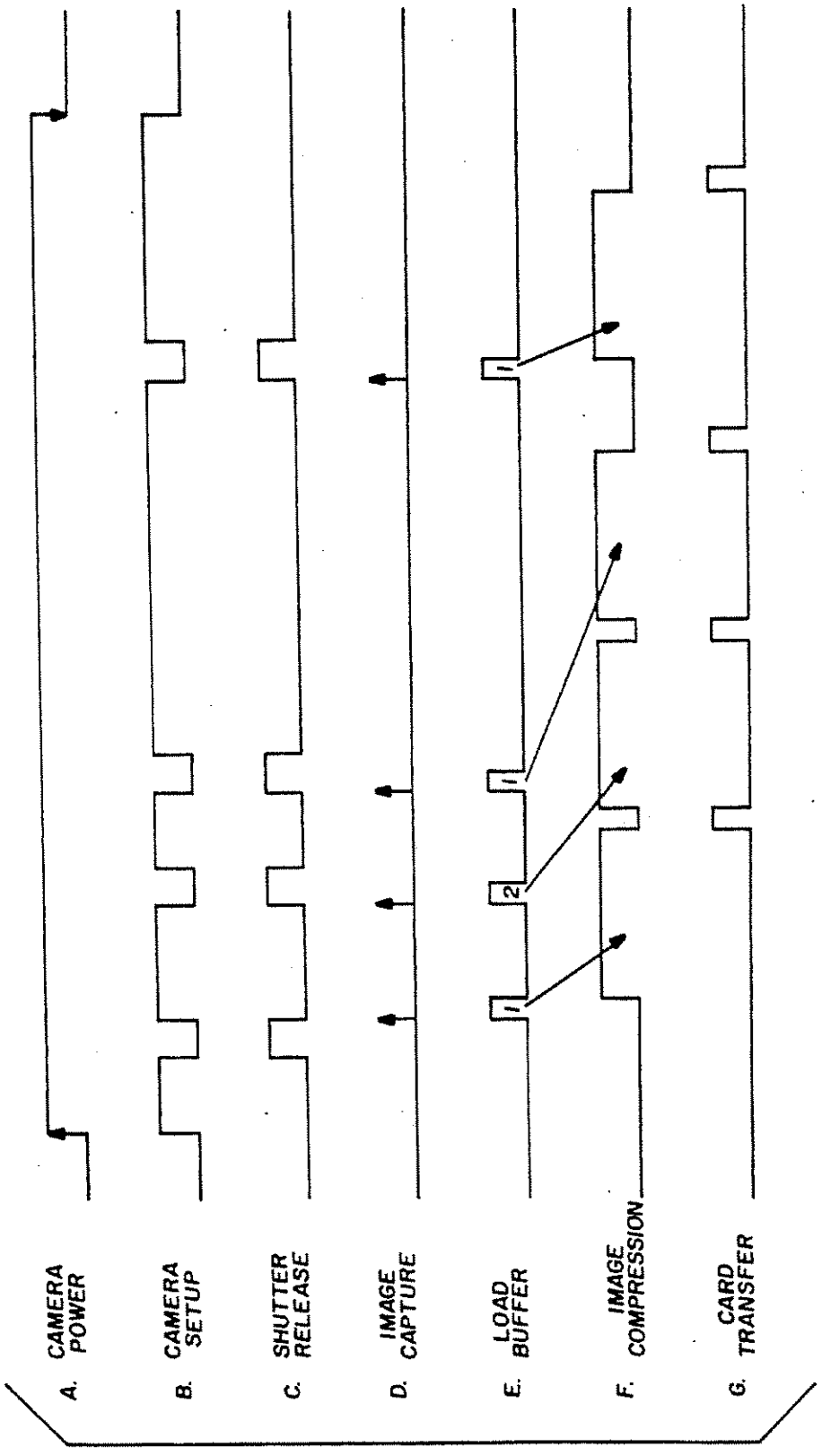


FIG. 2A

AX203264

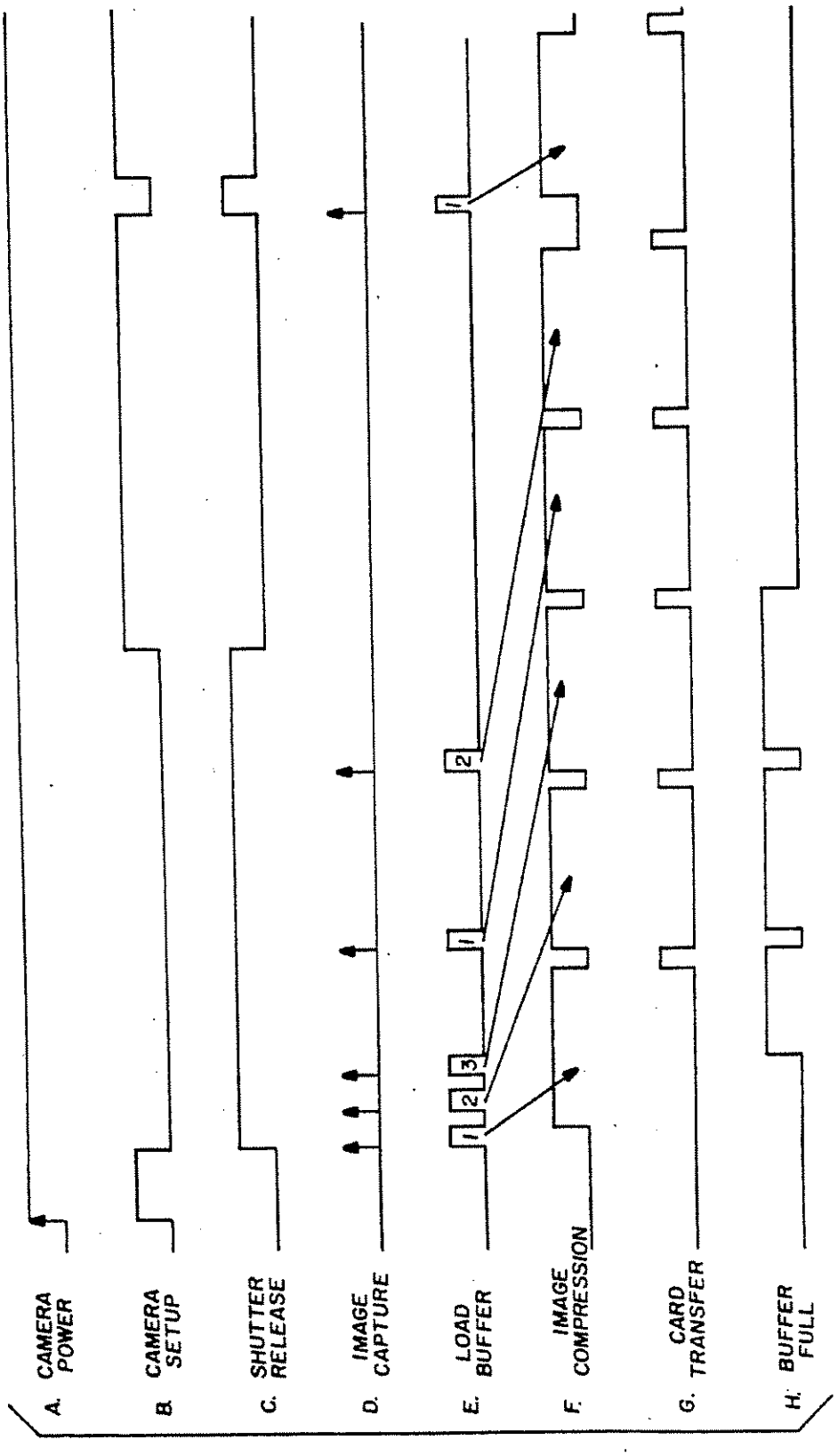

A. CAMERA POWER
B. CAMERA SETUP
C. SHUTTER RELEASE
D. IMAGE CAPTURE
E. LOAD BUFFER
F. IMAGE COMPRESSION
G. CARD TRANSFER
H. BUFFER FULL
1
2
3

FIG. 2B

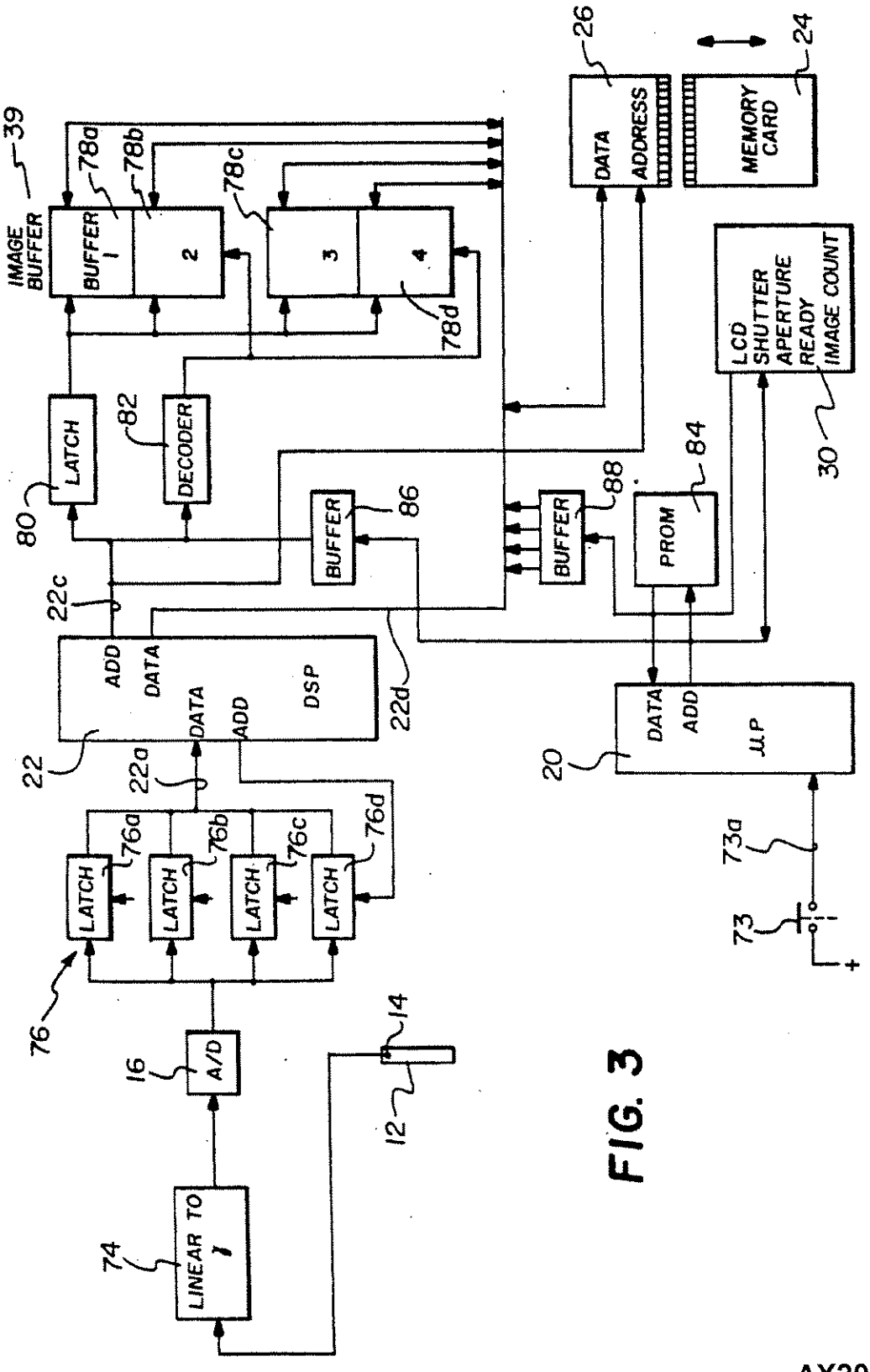

39
IMAGE BUFFER
78a
78b
78c
78d
BUFFER 1
2
3
4
26
DATA
ADDRESS
24
MEMORY CARD
LCD
SHUTTER
APERTURE
READY
IMAGE COUNT
30
LATCH
80
82
DECODER
BUFFER
86
BUFFER
88
84
PROM
22c
ADD
DATA
DATA
ADD
DSP
22
22d
22a
DATA
ADD
μP
20
76a
76b
76c
76d
LATCH
LATCH
LATCH
LATCH
76
73a
73
16
A/D
14
12
74
LINEAR TO

FIG. 3

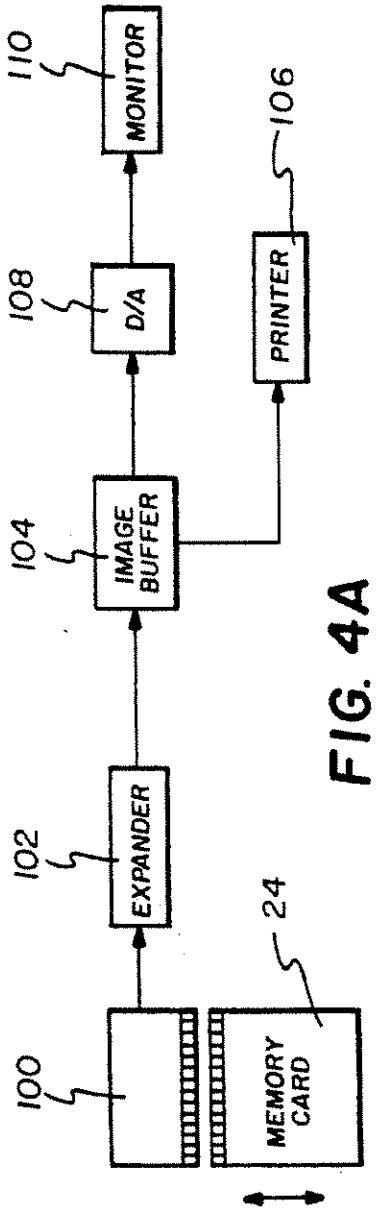

100
MEMORY CARD
24
102
EXPANDER
104
IMAGE BUFFER
106
PRINTER
108
D/A
110
MONITOR

FIG. 4A

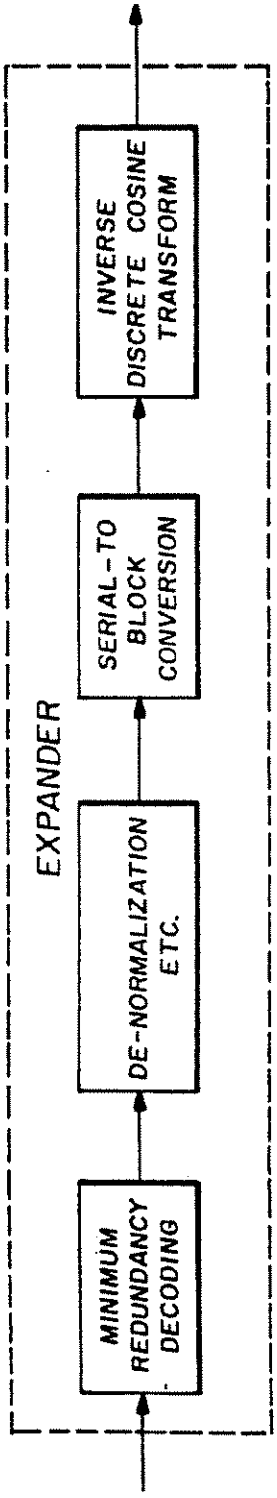

EXPANDER
MINIMUM REDUNDANCY DECODING
DE-NORMALIZATION ETC.
SERIAL-TO BLOCK CONVERSION
INVERSE DISCRETE COSINE TRANSFORM

FIG. 4B

ELECTRONIC STILL CAMERA UTILIZING IMAGE COMPRESSION AND DIGITAL STORAGE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention pertains in general to the field of electronic still imaging and, more particularly, to an electronic camera incorporating digital processing of image signals derived from an electronic image sensor and digital storage of the processed signals in a removable storage medium.

2. Description Relative to the Prior Art

An electronic still camera employing non-volatile storage of digital image signals is described in U.S. Pat. No. 4,489,351. Analog color information from three charge-coupled device (CCD) image sensors is converted into a digital bit stream and transmitted through a peripheral memory control unit to an integrated circuit memory. The memory is one unit of many, e.g., twenty-four memory units, recessed into a "cassette" that is separably attached through an electrical connector to the camera body. In order to obtain a digital image of high quality, many pixels, and thus many bits of digital information, need to be processed in a short time. In an article entitled "Possibilities of the Digital Electronic Still Camera", by Sumihisa Hashiguchi (*Shashin Kogaku*, pp. 110–111, Feb. 1988), the author proposes a multi-layer image processing integrated circuit including sensors, analog-to-digital (A/D) converters, and 8-bit buffer storage cells in respective layers. Since the output signal from an individual pixel is transferred "vertically" through an A/D converter to an included storage cell, real-time throughput is obtained without high speed operation. The stored signals can be read out slowly for digital recording, perhaps after compression, on a storage drive incorporating a small floppy disk. (Another example of a digital-based electronic still camera is shown in published UK Patent Application 2089169, in which the camera loads the digital image signals into a bubble memory cassette.)

A static random access memory (SRAM) card, in the size, and form, of a credit card, is an attractive storage alternative to the devices described in the above-related disclosures. For instance, published European Patent Application 289,944 shows a detachable SRAM module for use in a digital electronic still camera. The module is disclosed as a 32 M-bit (4 M-byte) SRAM integrated circuit card, although such storage capacities in a card are not commonly available at this time. A 512 K-byte SRAM card is presently available (Mitsubishi Electronics America, Inc. is one supplier). However, as pointed out in an article by Sumihisa Hashiguchi ("Picture Recording and Electric Power Consumption," *Shashin Kogyo*, pp. 94–95, Apr. 1988), there is a significant problem with memory volume. In the case, for example, of recording 780×490 picture elements from a CCD image sensor, with 8 bits allocated to each picture element, 382,200 bytes are required for a single monochrome video frame. This amounts to only one picture on a memory card (of 512 K-bytes). This is a considerable obstacle since still photographers are used to taking many pictures, e.g., 24 or 36 pictures, with one cassette of conventional film. Moreover, color pictures would ordinarily require three times the storage capacity of monochrome pictures.

Dynamic random access memory (DRAM) offers more storage in a reasonable volume, but power consumption quickly becomes formidable as storage capacity increases. The Hashiguchi article, consequently, calls for the development of new techniques of storage based on the compression of picture information by a factor of 10 or 100. As Hashiguchi points out, several picture compression techniques are available at present. For example, the aforementioned European Patent Application 289,944 suggests an embodiment in which a signal processor is adapted to accomplish data compression, such as the Hadamard transform, cosine transform or orthogonal transform, and coding on the video signal, which in turn is transferred to and stored interest that U.S. Pat. No. 4,131,919, which issued on Dec. 26, 1978, proposes the use of source and/or channel encoding schemes to more efficiently record digital still image signals on magnetic tape.) Adaptive differential pulse code modulation is another known compression algorithm for encoding still images.

The fundamental structure for in-camera digital processing is ordinarily based on a conventional analog camera, with digital processing techniques being applied to the functional analog blocks, such as color separation, white balance, gamma correction, and so on. This conventional transposition extends to real-time processing in that in-camera digital processing seeks, insofar as possible, to emulate real-time analog processing rates by rapidly accessing the imager, processing the resultant image signals, and writing the processed image signals to memory within normal video frame rates. (. . . albeit, that in the aforementioned *Shashin Kogaku* article of Feb. 1988, in U.S. Pat. No. 4,489,351, and in UK Patent Application 2089169, a buffer or temporary memory is provided to allow transmission of the image data to the recording device at a desired rate, which due to device or other limitations is often less than the image capture rate.) Nonetheless, as recognized by the Hashiguchi article, the available techniques neither adequately meet the requirement for real-time processing as needed by an electronic still camera nor the requirement for simply including the compression hardware with the camera.

SUMMARY OF THE INVENTION

The problem with the available techniques is their focus on real-time throughput. The present invention departs from this focus by distinguishing the input function of the camera from the processing function so that, on the one hand, image signals from a plurality of still images accumulate at a rate commensurate with normal operation of the camera while, on the other hand, the accumulated image signals are digitally processed at a throughput rate different than the accumulating rate. The prior techniques tend, by nature of their focus upon speed, not only to direct compression choices to those capable of handling a data stream at an extremely fast rate, such as differential pulse code modulation (DPCM), but also tend to focus processing upon one image at a time. By providing a multi-image input buffer and separating digital processing from input requirements, the digital processor not only has more time to operate on blocks of image signals, in particular transform encoding the blocks of signals, but also obtains such processing advantages without disturbing the "stacking up" of images in the input buffer. The invention further utilizes a removable digital storage means, such as a SRAM memory card, to store the compressed image signals. With 10:1 compression, for example, the

byte requirement for a picture can be reduced by a factor of ten and many more images can be stored in the memory card.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in relation to the drawings, in which:

FIG. 1A is a block diagram of an electronic still camera employing digital processing according to the invention;

FIG. 1B is a block diagram of an exemplary form of image compression used in connection with the invention;

FIG. 2A is a functional sequence diagram showing multi-image input buffering;

FIG. 2B is a further functional sequence diagram showing full utilization of the input buffer and concomitant delay;

FIG. 3 is a block diagram showing details of a specific processing architecture for the electronic still camera;

FIG. 4A is a block diagram of an electronic still player for use in reproducing pictures taken with the camera of FIG. 1A; and

FIG. 4B is a block diagram of an exemplary form of image expansion used in connection with the player of FIG. 4A.

DETAILED DESCRIPTION OF THE INVENTION

Because electronic still cameras employing charge-coupled device (CCD) sensors are well known, the present description will be directed in particular to elements forming part of, or cooperating more directly with, apparatus in accordance with the present invention. Elements not specifically shown or described herein may be selected from those known in the art.

Referring initially to FIGS. 1A and 1B, an electronic still camera is divided generally into an input section 2 and a compression and recording section 4. The input section 2 includes an exposure section 10 for directing image light from a subject (not shown) toward an image sensor 12. Although not shown, the exposure section 10 includes conventional optics for directing the image light through a diaphragm, which regulates the optical aperture, and a shutter, which regulates exposure time. The sensor 12, which includes a two-dimensional array of photosites corresponding to picture elements of the image, is a conventional charge-coupled device (CCD) using either well-known interline transfer or frame transfer techniques. The sensor 12 is exposed to image light so that analog image charge information is generated in respective photosites. The charge information is applied to an output diode 14, which converts the charge information to analog image signals corresponding to respective picture elements. The analog image signals are applied to an A/D converter 16, which generates a digital image signal from the analog input signal for each picture element.

The digital signals are applied to an image buffer 18, which is a random access memory (RAM) with storage capacity for a plurality of still images. The arrangement for allocating memory space in the image buffer 18 to individual frames may vary; for this description, however, the frames will be allocated to specific, identifiable memory spaces such that a new frame can be directly written over an old frame without affecting the other frames in the buffer 18. This, as will be shown, becomes convenient in unloading the buffer 18 and freeing memory space for a new frame as soon as the older ones are processed.

A control processor 20 generally controls the input section 2 of the camera by initiating and controlling exposure (by operation of the diaphragm and shutter (not shown) in the exposure section 10), by generating the horizontal and vertical clocks needed for driving the sensor 12 and for clocking image information therefrom, and by enabling the A/D converter 16 in conjunction with the image buffer 18 for each signal segment relating to a picture element. (The control processor 20 would ordinarily include a microprocessor coupled with a system timing circuit.) Once a certain number of digital image signals have been accumulated in the image buffer 18, the stored signals are applied to a digital signal processor 22, which controls the throughput processing rate for the compression and recording section 4 of the camera. The processor 22 applies a compression algorithm to the digital image signals, and sends the compressed signals to a removable memory card 24 via a connector 26. A representative memory card is a 512 K-byte static random access memory (SRAM) available from Mitsubishi Corp.

Since the compression and related processing ordinarily occurs over several steps, the intermediate products of the processing algorithm are stored in a processing buffer 28. (The processing buffer 28 may also be configured as part of the memory space of the image buffer 18.) The number of image signals needed in the image buffer 18 before digital processing can begin depends on the type of processing, that is, for a block transformation to begin, a block of signals including at least a portion of the image signals comprising a video frame must be available. Consequently, in most circumstances, the compression may commence as soon as the requisite block, e.g., of 16×16 picture elements, is present in the buffer 18.

The input section 2 operates at a rate commensurate with normal operation of the camera while compression, which consumes more time, can be relatively divorced from the input rate. The exposure section 10 exposes the sensor 12 to image light for a time period dependent upon exposure requirements, for example, a time period between 1/1000 second and several seconds. The image charge is then swept from the photosites in the sensor 12, converted to a digital format, and written into the image buffer 18 during a standard rate, which may, for example, correspond to a standard video field or frame rate. The repetition rate of the driving signals provided by the control processor 20 to the sensor 12, the A/D converter 16 and the buffer 18 are accordingly generated to achieve such a transfer. The processing throughput rate of the compression and recording section 4 is determined by the character of an image, i.e., the amount of detail versus redundant information, and the speed of the digital signal processor 22, and may take up to several seconds for an especially complex image.

One desirable consequence of this architecture is that the processing algorithm employed in the compression and recording section may be selected for quality treatment of the image rather than for throughput speed. This, of course, can put a delay between consecutive pictures which may affect the user, depending on the time between photographic events. This is a problem since it is well known and understood in the field of still video recording that a digital still camera should pro-

vide a continuous shooting capability for a successive sequence of images. For this reason, the image buffer **18** shown in FIG. **1** provides for storage of a plurality of images, in effect allowing a series of images to "stack up" at video rates. The size of the buffer is established to hold enough consecutive images to cover most picture-taking situations. FIGS. **2A** and **2B** show the typical functional sequence for a camera having buffer area for three separate images. As each image is captured (line D), the next available buffer area is loaded (line E) and image compression begins (line F). FIG. **2A** illustrates a typical situation in which the shutter release (line C) is actuated at spaced times insufficient to load all three buffer areas. In FIG. **2B**, the shutter release is continuously held down (line C) and a burst of exposures ensue. The three buffer areas are quickly loaded (line E) and, responsive to a buffer full signal (line H), the control processor **20** interrupts the exposure section **10**. No further image is then captured until a buffer is freed. For example, in lines E and F, after the first image is compressed and transferred to the card **24**, the first buffer area is freed up and a fourth exposure is made.

An operation display panel **30** is connected to the control processor **20** for displaying information useful in operation of the camera. Such information might include typical photographic data, such as shutter speed, aperture, exposure bias, color balance (auto, tungsten, fluorescent, daylight), field/frame, low battery, low light, exposure modes (aperture preferred, shutter preferred), and so on. Moreover, other information unique to this type of camera is displayed. For instance, the memory card **24** would ordinarily include a directory signifying the beginning and ending of each stored image. This would show on the display **30** as either (or both) the number of images stored or the number of image spaces remaining, or estimated to be remaining.

The control processor **20** also accesses a card diagnostics memory **31** for generating important information about the condition of the memory card **24**. Specifically, the connector **26** is queried for the presence of a card **24** and, if no card is connected, a "no card" display is produced on the operation display **30**. Likewise, if a card is present but it is full of images, a "card full" display is produced. The card diagnostics memory **31** also provides a verification routine to check the card **24** for faults or defects. For instance, a set of code patterns (such as 010101 . . . and 101010 . . .) can be written into and read from the card to verify memory locations. This is especially important since compressed data is stored on the card **24** and even one defective memory location can produce an extensive visual artifact in the expanded picture. If a card **24** fails the verification test, a "defective card" display is produced on the operation display **30**.

Buffer diagnostics are maintained in a memory **32** for producing certain information about the condition of the image buffer **18**. Its principal purpose is to monitor the utilization of buffer space and produce, as shown in line H of FIG. **2B**, a "buffer full" signal when no more buffer space is available. A corresponding display is produced on the display **30**, which is important to the user as no further image can be captured until a buffer area is freed up. The digital signal processor **22** further provides a signal indicative of the compression operation on a line **30***a* to the operation display **30**, that is, a signal indicating that compression is underway. A corresponding display, "compression underway", is activated by the display **30**.

The digital signal processor **22** compresses each still video image stored in the image buffer **18** according to a known image compression algorithm shown in FIG. **1B**. The compression algorithm begins with a discrete cosine transformation (block **33**) of each successive block of the image data to generate a corresponding block of cosine transform coefficients. It is well-known that compression techniques are greatly enhanced when applied to image data which has been previously transformed in accordance with a discrete cosine transform algorithm. The cosine transform coefficients are then rearranged in serial order by a block-to-serial conversion step (block **34**) described and illustrated in U.S. Pat. No. 4,772,956, "Dual Block Still Video Compander Processor," issued Sept. 20, 1988 to Roche et al., and which is assigned to the assignee of the present invention and incorporated by reference into the present patent application. The block-to-serial conversion step consists of arranging the discrete cosine transform coefficients in order of increasing spatial frequency, which corresponds to a zig-zag pattern illustrated in the Roche et al patent. The resulting serial string of transform coefficients is then subjected to thresholding, normalization, and quantization (block **36**) and minimum redundancy encoding (block **38**).

Thresholding discards data words of magnitudes less than a threshold number. Normalization entails dividing each data word by a divisor to yield a quotient. Quantization discards the fractional bits in the quotient. Minimum redundancy encoding is a technique well-known in the prior art and employs two complimentary steps, namely amplitude encoding and run length encoding. Amplitude encoding (or "Huffman Encoding") assigns to each of a finite set of possible amplitudes an encoded bit pattern designed to require the smallest number of bits for non-redundant representation. Run length encoding represents any consecutive run of zeros in the data as the smallest non-redundant bit pattern required to count the number of zeros in the run. The set of bit patterns representing each of the possible word amplitudes and the set of bit patterns representing each of the possible zero run lengths may be selected in accordance with the well-known principles and stored in look-up tables for use during the compression process. This compression technique greatly reduces the number of bits required to represent a frame of still video information, without reduction in image quality, thereby greatly reducing the amount of storage that must be allocated to each still frame in the SRAM card **24**.

The uncompressed still video data stored in the image buffer **18** is organized in the manner of a television picture, that is, in vertical columns and horizontal rows of video data bytes (representing the corresponding picture elements) divisible into square blocks of bytes, each block comprising, e.g., 16 columns and 16 rows of bytes. The control processor **20** fetches a block of data each time the digital signal processor **22** is about to execute the compression algorithm. The compression process eliminates many bits contained in each block of video data, so that the compressed video data does not emerge from the processor **22** as a standard-length stream of bits, but as a variable number of bits dependent upon the complexity of the picture and the rules used for truncating bits. The memory space, therefore, allocated for each image in the SRAM card **24** can vary from image to image. The processor **22**, consequently,

allocates memory space in the SRAM card **24** after each compression sequence for an image is completed so that the images may be "packed" into the card as a continuum of compressed image data. This means the storage capacity, in terms of actual images, of the SRAM card is unknown in the beginning, and then gradually is specified as pictures are taken and the card is "filled". The control processor **20** monitors the numbers of images, furnishing a running total to the operation display panel **30**, and further triggers a special "one more picture" display when the remaining memory space is sufficient for a predetermined number of, say one more, pictures. Alternatively, a fixed "maximum" space can be allocated in the SRAM card **24** for each image; in this case, fewer images can be stored although the total capacity is always known.

What has been described to this point applies equally to monochrome or color pictures, except that color pictures require additional processing. For instance, if a multi-spectral color filter array (shown in broken line **40** in FIG. **1A**) overlies the image sensor **12**, the various colors are sorted out and processed differently for each color. This would be accomplished by an additional routine in the digital signal processor **22**. Such color filter array processing would precede the discrete cosine transform block **33** (FIG. **1B**) so that image compression can be done separately on each color and three compressed frames would be stored in the memory card **24** for each image.

FIG. **3** illustrates details of a specific processing architecture in which an image buffer **39** combines the function of the image buffer **18** and the processing buffer **28** shown in FIG. **1A**. The analog signals from the output diode **14** of the image sensor **12** are gamma-corrected in a conventional linear-to-gamma correction circuit **74** and applied to the A/D converter **16**. The output of the A/D converter **16** is connected to an 8 bit-to-32 bit latching array **76** comprising latches **76***a*, **76***b*, **76***c*, and **76***d*. In practice, the latching array **76** performs a double buffering operation to save time, that is, the latched bytes are unloaded in pairs to the processor **22** on a 32 bit-wide input data bus **22***a*, as follows. After latches **76***a* and **76***b* are loaded with the first two bytes provided by the A/D converter **16**, the latched bytes are applied in parallel to the data bus **22***a*. In the meantime other two latches **76***c* and **76***d* are being loaded with the next two bytes. When the latches **76***c* and **76***d* are full, the latched bytes are applied in parallel to the input data bus **22***a* while the other latches **76***a* and **76***b* are being loaded with new bytes.

In this architecture, therefore, the digital signal processor **22** has the initial function, prior to compression, of transferring the paired input bytes to the image buffer **39**, which includes random access memories (RAMs) **78***a*, **78***b*, **78***c*, and **78***d*. In terms of allocating bytes to storage, RAM **78***a* receives data from the latch **76***a*, RAM **78***b* from latch **76***b*, and so on. The digital signal processor **22** produces address words on an address bus **22***c* connected to the RAMs **78***a*–**78***d*. The address word is held in an address latch **80** while a portion of the address word is decoded in a decoder **82** for activating the appropriate chip enable ports of the image buffer RAMs **78***a*–**78***d*. As shown in FIG. **3**, the buffer **39** is enabled in pairs of RAMs **78***a*–**78***d* to correspond to the paired bytes being transferred from the latches **76***a*–**76***d*.

The embodiment of FIG. **3** includes no resident non-volatile memory for the digital processor **22**. Consequently, the operating program code for the camera is stored in a programmable read only memory (PROM) **84** connected to the address and data buses of the control processor **20**. These bus lines are also connected, through respective buffers **86** and **88**, to the output address bus **22***c* and the output data bus **22***d* of the digital processor **22**. The control processor **20** downloads portions of the operating program from the PROM **84** to the image buffer **39** as required for operation of the digital processor **22**. For instance, when a shutter release **73** is depressed and a line **73***a* is activated, the control processor **20** downloads the data acquisition code over the data bus **22***d* to a specified location in the image buffer **39**. The appropriate address words are then applied to the address bus **22***c* by the control processor **20** and the operating code is written into volatile memory in the digital processor **22**. The processor **22** is then ready to latch incoming image bytes into the latch array **76** and transfer paired bytes to the image buffer **39**.

When all the image bytes of a still picture are in the image buffer **39**, the control processor **20** downloads the operating code for the discrete cosine transform from the PROM **84** to a specified unused memory space in the image buffer **39**. The DCT code is written into the volatile memory of the processor **22** and the discrete cosine transformation is performed on blocks of image bytes in the image buffer **39**. After each block is transformed, the transform coefficients are written back into the image buffer **39**. The control processor **20** next downloads the operating code for the block to serial conversion in like manner, the conversion is performed, and the serial string is written back into the buffer. Then the code for thresholding, normalization and quantization is downloaded in similar fashion, the processing done and processed data stored, and the code for minimum redundancy encoding is downloaded and the amplitude and run length encoding is done. With the image data now in its finally compressed form, and instead of writing the compressed data back into the buffer **39** one more time, the compressed data is directly written into the memory card **24**. The above-related technique for storing the operating code in the PROM **84** and downloading sections thereof as needed conserves on the need for fast, and therefore expensive, non-volatile memory dedicated to the processor **22**.

A simplified block diagram is shown in FIG. **4***a* of a still video player for reproducing a picture or for making a hard copy print from the digital image signals stored in compressed format in the memory card **24**. With the card **24** inserted into a connector **100**, the digital signals are accessed and processed in an expander **102**. An expansion algorithm, which is basically the inverse of the compression algorithm of FIG. **1B**, is shown in FIG. **4B** and implemented by the expander **102**. The digital image data is expanded block-by-block and stored in an image buffer **104** as a decompressed image. A conventional thermal printer **106** is connected to the buffer **104** for making a hard copy thermal print from the decompressed image. In addition, the decompressed image signals are converted to analog form by a digital-to-analog (D/A) converter **108** and displayed on a conventional CRT monitor **110**.

The invention has been described in detail with particular reference to a presently preferred embodiment, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

What is claimed is:

1. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said imaging apparatus including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image information if generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to the picture elements;

an image buffer with storage capacity for storing digital image signals corresponding to a plurality of still images;

control processor means responsive to user instructions for initiating operation of said exposing means, for clocking the image information from said sensor, and for controlling said converting means to deliver said digital signals to said image buffer, said control processor means loading digital image signals corresponding to said plurality of still images into said image buffer at an input rate commensurate with normal operation of the camera;

digital processing means for operating on blocks of stored digital image signals at a processing throughput rate different than said input rate, said digital processing means including means for transforming blocks of digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a compressed stream of processed digital image signals;

means responsive to said digital processing means for downloading the processed image signals to said removable digital memory; and

diagnostic means for monitoring the utilization of said image buffer whereby information is generated as to the current condition of the image buffer.

2. The apparatus claimed in claim 1 in which said diagnostic means includes means for monitoring the remaining storage capacity of said image buffer.

3. The apparatus as claimed in claim 2 in which said diagnostic means includes means for providing a buffer full signal when said buffer is fully loaded.

4. The apparatus as claimed in claim 3 wherein said control processor means includes means responsive to said buffer full signal for interrupting said exposing means and preventing further exposure of said image sensor.

5. The apparatus as claimed in claim 3 further including a visual indicator and wherein said control processor means activates said visual indicator according to the state of said buffer full signal.

6. The apparatus as claimed in claim 1 in which said digital processing means further includes a processing buffer, said digital processing means operating on blocks of digital image signals before said image buffer is fully loaded and storing intermediate products of said processing in said processing buffer so that memory space is freed in said image buffer for further storage of new still images.

7. The apparatus as claimed in claim 1 which said digital processing means generates in operating signal indicating when the compression algorithm is operating.

8. The apparatus as claimed in claim 7 further including a visual indicator and wherein said control processor means activates said visual indicator according to the state of said operating signal.

9. The apparatus as claimed in claim 1 in which said digital processing means compresses the digital image signal in a plurality of stages, one stage including the performance of a discrete cosine transform on the blocks of image signals and another stage including minimum redundancy encoding of the transformed image signals.

10. An electronic still camera employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said camera including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image signals are obtained from the respective photosites, said camera comprising:

an A/D converter for converting the analog image signals into digital image signals;

a digital processor for processing the digital image signals through a compression algorithm and for generating a stream of compressed signals having a variable bit length dependent upon the character of the image, said processor allocating a variable-length memory space in said removable digital memory for each image;

means for downloading the compressed signals to the allocated image space such that consecutive memory spaces may differ in length depending on the character of each image; and

means for generating a warning signal when the remaining unused memory space in said removable digital memory corresponds to a predetermined amount of memory space generally suitable for at least one more still image.

11. The camera as claimed in claim 10 further including a visual indicator and means for activating said visual indicator according to the state of said warning signal.

12. An electronic still camera employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said camera including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image signals are obtained from the respective photosites, said camera comprising:

an A/D converter for converting the analog image signals into digital image signals;

a random access image buffer having memory space sufficient for a plurality of still images;

control means responsive to repeated actuation of said exposing means for entering the digital image signals corresponding to a sequence of still images into said image buffer at a rate commensurate with normal operation of the camera, said control means intermittently disabling and reenabling said exposing means according to the memory space remaining in said random access image buffer;

a digital processor for compressing the digital image signals, said processor connected to said buffer for operating on stored digital signals from the first stored image irregardless of the entering of digital

signals corresponding to subsequent still images into said buffer; and

means responsive to said digital processor for downloading the compressed image signals to said removable digital memory.

13. The camera as claimed in claim 12 in which said digital processor operates a compression algorithm on blocks of stored digital signals corresponding to blocks of picture elements, said block compression operating irregardless of the entering of digital signals corresponding to further blocks of the same image.

14. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said imaging apparatus including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to the picture elements;

an image buffer with storage capacity for storing digital image signals corresponding to a plurality of still images;

control processor means responsive to user instructions for initiating operation of said exposing means, for clocking the image information from said sensor, and for controlling said converting means to deliver said digital signals to said image buffer, said control processor means loading digital image signals corresponding to said plurality of still images into said image buffer at an input rate commensurate with normal operation of the camera;

digital processing means for operating on blocks of stored digital image signals at a processing throughput rate different than said input rate, said digital processing means including means for transforming blocks of digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a compressed stream of processed digital image signals;

means responsive to said digital processing means for downloading the processed image signals to said removable digital memory; and

diagnostic means for checking the removable digital memory for faults or defects.

15. The apparatus as claimed in claim 14 in which said diagnostic means includes means for providing a defective card signal whenever the removable digital memory fails the check provided by said diagnostic means.

16. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said imaging apparatus including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to the picture elements;

an image buffer for storing one or more blocks of digital image signals corresponding to portions of a still image;

control processor means responsive to user instructions for initiating operation of said exposing means, for clocking the image information from said sensor, and for controlling said converting means to deliver said digital signals to said image buffer;

digital processing means for operating on each block of stored digital image signals, said digital processing means including means for transforming each block of digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a compressed stream of processed digital image signals;

diagnostic means for checking the removable digital memory for faults or defects and for providing an indication thereof; and

means responsive to said digital processing means and to said indication from said diagnostic means for downloading the processed image signals to said removable digital memory.

17. The apparatus as claimed in claim 16 in which said diagnostic means includes means for providing a defective card warning signal whenever the removable digital memory fails the check provided by said diagnostic means.

18. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said imaging apparatus including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said area image sensor including a color filter array having a multi-colored pattern oriented to said photosites and including one color representative of luminance, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to the picture elements;

an image buffer with storage capacity for storing digital image signals corresponding to a plurality of still images;

control processor means responsive to user instructions for initiating operation of said exposing means, for clocking the image information from said sensor, and for controlling said converting means to deliver said digital signals to said image buffer, said control processor means loading digital image signals corresponding to said plurality of still images into said image buffer at an input rate commensurate with normal operation of the camera;

digital processing means for operating on blocks of stored digital image signals at a processing throughput rate different than said input rate, said digital processing means including means for transforming blocks of digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a compressed stream of processed digital image signals, said digital processing means interpolating at least the luminance component over the block area and transforming each block of digital signals including the interpolated signals; and

means responsive to said digital processing means for downloading the processed image signals to said removable digital memory.

* * * * *

EXHIBIT 49

US005164831A

United States Patent [19]

Kuchta et al.

[11] Patent Number: 5,164,831

[45] Date of Patent: Nov. 17, 1992

[54] ELECTRONIC STILL CAMERA PROVIDING MULTI-FORMAT STORAGE OF FULL AND REDUCED RESOLUTION IMAGES

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[73] Assignee: Eastman Kodak Company, Rochester, N.Y.

[21] Appl. No.: 494,205

[22] Filed: Mar. 15, 1990

[51] Int. Cl.[5] H04N 5/30

[52] U.S. Cl. 358/209; 358/102; 358/909; 358/432; 360/35.1

[58] Field of Search 358/432, 909, 906, 403, 358/433, 445, 447, 448, 452, 458, 133, 459, 209, 471, 102; 360/33.1, 35.1

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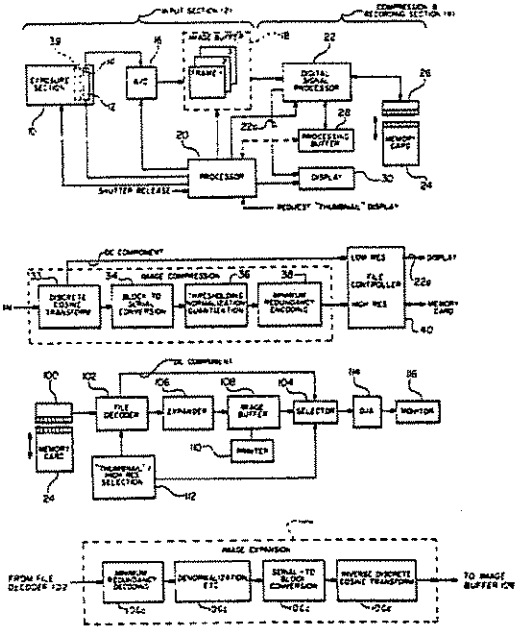
Assistant Examiner—Jeffrey S. Murrell
Attorney, Agent, or Firm—David M. Woods

[57] ABSTRACT

An electronic still camera employs digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable static random access memory card. An image sensor is exposed to image light and the resultant analog image information is converted to digital image signals. A control processor controls the exposure section and the A/D converter, delivering digital signals to a multi-image buffer at a rate commensurate with normal operation of the camera. A digital processor operates on the stored digital signals, transforming blocks of the digital signals and encoding the signals into a compressed stream of processed image signals, which are downloaded to the memory card. The digital processor operates at a throughput rate different than the input rate for better image capture and optimum utilization of the camera.

15 Claims, 3 Drawing Sheets



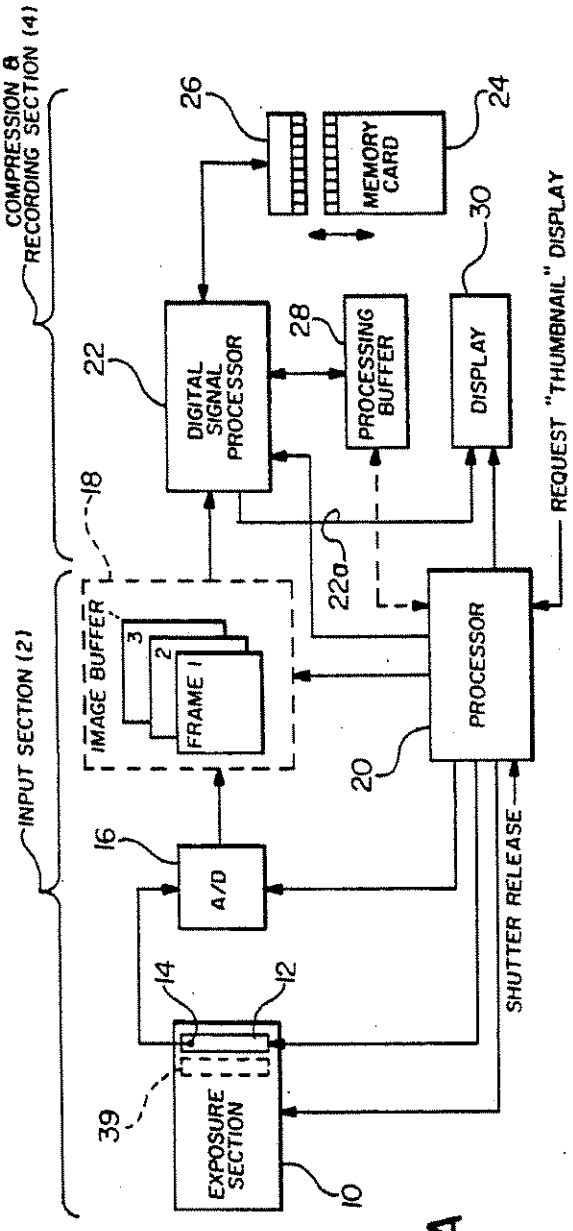

COMPRESSION & RECORDING SECTION (4)
INPUT SECTION (2)
IMAGE BUFFER
FRAME 1
2
3
A/D
EXPOSURE SECTION
DIGITAL SIGNAL PROCESSOR
PROCESSING BUFFER
DISPLAY
MEMORY CARD
PROCESSOR
SHUTTER RELEASE
REQUEST "THUMBNAIL" DISPLAY
10
12
14
16
18
20
22
22a
24
26
28
30
39

FIG. IA

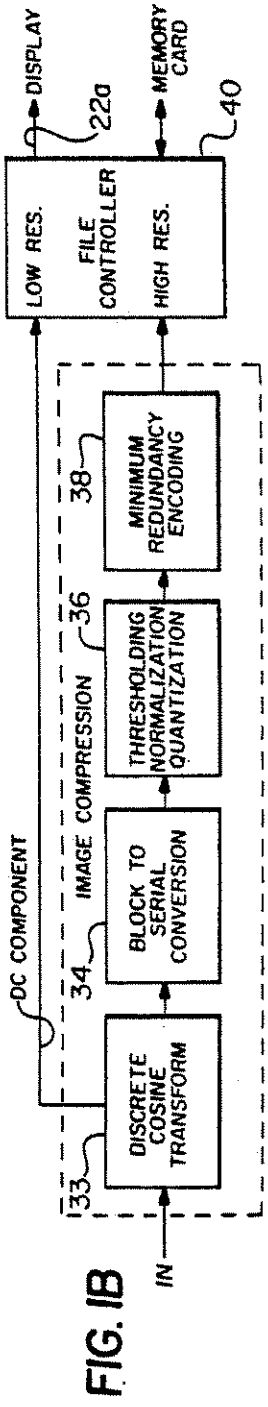

DISPLAY
MEMORY CARD
LOW RES.
FILE CONTROLLER
HIGH RES.
22a
40
DC COMPONENT
IMAGE COMPRESSION
DISCRETE COSINE TRANSFORM
BLOCK TO SERIAL CONVERSION
THRESHOLDING NORMALIZATION QUANTIZATION
MINIMUM REDUNDANCY ENCODING
33
34
36
38
IN

FIG. IB

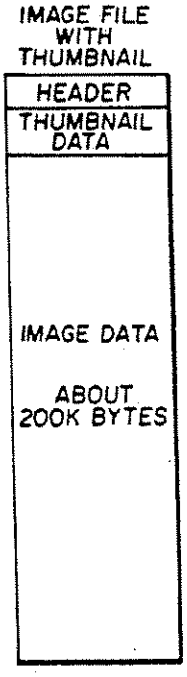


IMAGE FILE WITH THUMBNAIL
HEADER
THUMBNAIL DATA
IMAGE DATA
ABOUT 200K BYTES

FIG. 2A

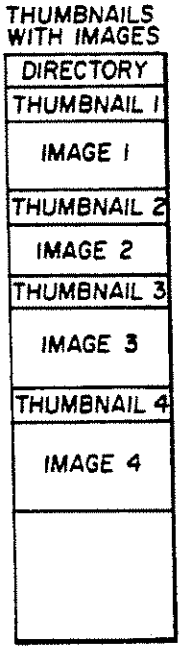

THUMBNAILS WITH IMAGES
DIRECTORY
THUMBNAIL 1
IMAGE 1
THUMBNAIL 2
IMAGE 2
THUMBNAIL 3
IMAGE 3
THUMBNAIL 4
IMAGE 4

FIG. 2B

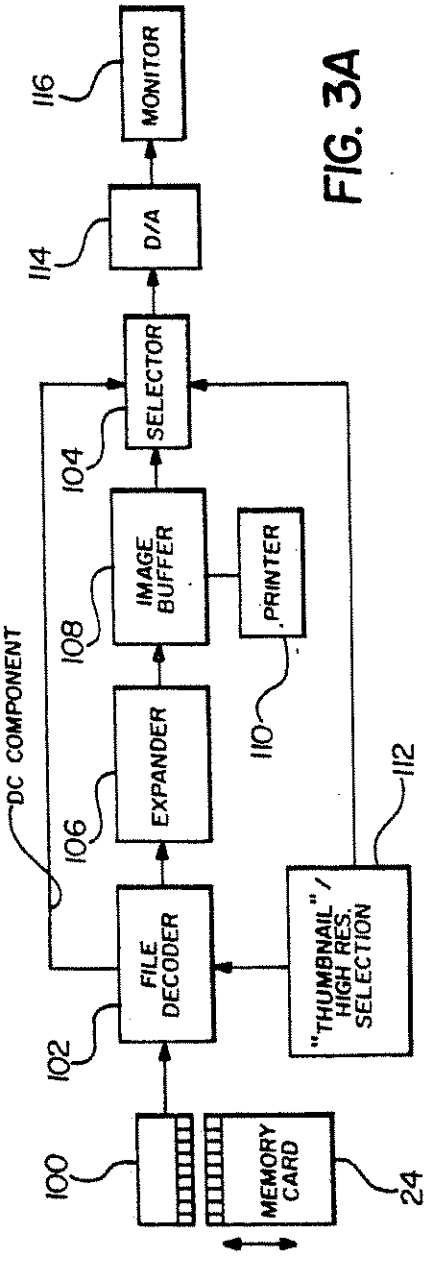


FIG. 3A

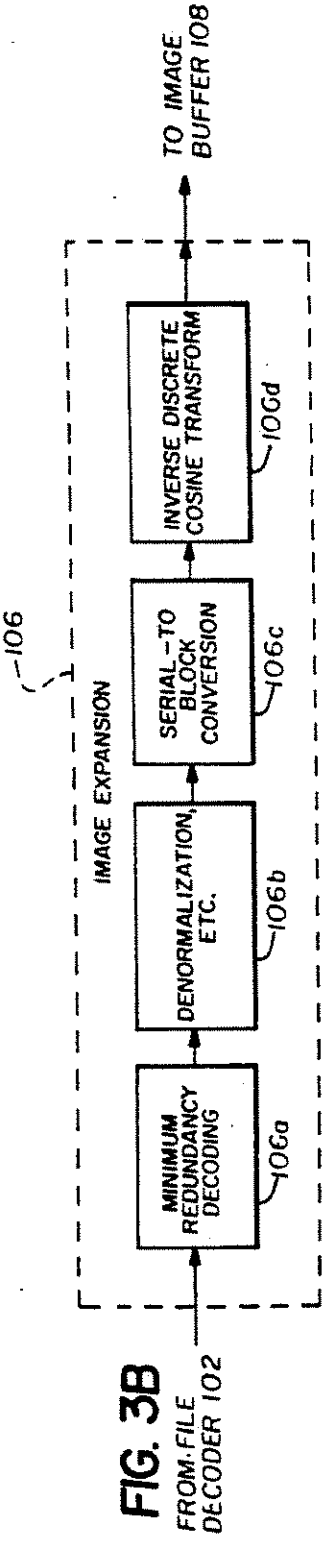


FIG. 3B

AX203277

ELECTRONIC STILL CAMERA PROVIDING MULTI-FORMAT STORAGE OF FULL AND REDUCED RESOLUTION IMAGES

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention pertains in general to the field of electronic still imaging and, more particularly, to apparatus incorporating digital processing of image signals derived from an electronic image sensor and digital storage of the processed signals.

2. Description Relative to the Prior Art

An electronic still camera employing non-volatile storage of digital image signals is described in copending U.S. patent application Ser. No. 349,566, filed May 9, 1989 now U.S. Pat. No. 5,016,107 dated May 1, 1991, and assigned to the same assignee as the present invention. The electronic still camera disclosed therein employs digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable static random access memory card. An image sensor is exposed to image light and the resultant analog image information is converted to digital image signals. The digital signals are delivered to a multi-image buffer at a rate commensurate with normal operation of the camera. A digital processor operates on the stored digital signals, transforming blocks of the digital signals and encoding the signals into a compressed stream of processed image signals, which are downloaded to the memory card. The digital processor operates at a throughput rate different than the input rate, thereby allowing more efficient image capture and optimum utilization of the camera.

Despite efficient operation of such a camera and the use of compression to reduce the amount of data, high quality digital image files written in the memory card are nonetheless quite large and take significant amounts of time to process due to image size, image resolution, and the nature of the compression process. For example, a 1,280 by 1,024 pixel, 24-bit per pixel image might compress over many seconds to 100 to 300 Kilobytes of storage area. It is often desirable to quickly review the images on the memory card before deciding to transmit, to make a copy, or to retake a picture. The physical time for decompression and display of a high resolution image can be so slow as to interfere with the review process.

The matter of electronic preview has been taken up in a number of prior art disclosures. For instance, in U.S. Pat. No. 4,827,347 an electronic still camera includes a Plurality (twelve) of small displays connected to a like plurality of display/framestores so that pictures can be previewed as a group and then individually retained or discarded. The aforementioned processing time problem, however, is not addressed. In U.S. Pat. No. 4,763,208, an electronic still camera cooperates with playback apparatus that subsamples images recorded on a disk and simultaneously displays the subsampled images as a group on a monitor. While with this construction the contents of the disk can be searched within a shorter time, the subsampled images are unavailable for subsequent review. Research Disclosure item 28618 (p. 71 of the February, 1988 issue) describes a concept for storing video signals from electronically scanned negatives on individual tracks of a video disk while simultaneously storing miniature versions of these pictures in a mosaic frame store. After all the images are recorded on their individual tracks, and the mosaic frame store is accordingly filled, the mosaic-like content of the frame store is itself recorded as a full NTSC frame on a separate track. A similar concept is applied to an all-video picture processing system in U.S. Pat. No. 4,802,019 for rearranging, replacing, or inserting video programs in a sequence of such programs. Each program is characterized by a single frame that is reduced or "squeezed" to one sixteenth its original size and included in a mosaic of like pictures on an index screen. Rearrangement, etc. of the video programs is then made by reference to the index screen. In the latter two systems, the miniaturized pictures are stored together as a video frame. This is of little aid in an all-electronic system in which the pictures are, for example, separately transmitted to a remote location, separately edited, or otherwise used in a way in which continued, rapid review of a particular recorded picture is desirable.

SUMMARY OF THE INVENTION

The invention is based on the addition of a reduced resolution image to the digital file format for an individual high resolution image. Particularly if the reduced resolution, or "thumbnail", image is created as a part of the image acquisition process, or in close timing thereto, it is convenient to provide multi-format storage of the "thumbnail" image in a reserved area associated with each image file. The "thumbnail" image then follows the high resolution image wherever the image file travels. Since the "thumbnail" image is easily and quickly accessed, reviewing and display is extremely fast.

In accordance with the invention, electronic still imaging apparatus employs digital processing of image signals corresponding to a still image and storage of the processed image signals in a digital memory. The imaging apparatus also includes an image sensor having an array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image information is generated in respective photosites. The analog image information is converted into digital image signals and, further, reduced resolution signals are generated from the digital image signals. A multi-format image file is formed by combining the (full resolution) digital image signals and the reduced resolution signals. The image file is then stored in the digital memory, where the reduced resolution signals may be quickly accessed for rapid display.

In accordance with a further embodiment of the invention, electronic still image processing apparatus includes an image buffer with storage capacity for storing digital image signals corresponding to a still image. A digital processor transforms blocks of the stored digital image signals into corresponding sets of transform coefficient signals and encodes the coefficient signals into a compressed stream of processed image signals. In addition, the digital processor generates reduced resolution image signals from the stored digital image signals and downloads both the processed (high resolution) image signals and the reduced resolution image signals to a digital memory. In a preferred implementation, the reduced resolution signals are based on the average or dc component coefficient signals generated during the transformation.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in relation to the drawings, in which:

FIG. 1A is a block diagram of an electronic still camera employing digital processing and multi-format storage according to the invention;

FIG. 1B is a block diagram of an exemplary form of image compression used in connection with the invention;

FIG. 2A is a diagram of a preferred file format for a single full resolution image and its associated "thumbnail" image;

FIG. 2B is a diagram of a preferred file format for several full resolution images and their associated "thumbnail" images;

FIG. 3A is a block diagram of an electronic still player for use in reproducing pictures taken with the camera of FIG. 1A; and

FIG. 3B is a block diagram of an exemplary form of image expansion used in connection with the player of FIG. 3A.

DETAILED DESCRIPTION OF THE INVENTION

Because electronic still cameras employing charge-coupled device (CCD) sensors are well known, the present description will be directed in particular to elements forming part of, or cooperating more directly with, apparatus in accordance with the present invention. Elements not specifically shown or described herein may be selected from those known in the art.

Referring initially to FIGS. 1A and 1B, an electronic still camera is divided generally into an input section 2 and a compression and recording section 4. The input section 2 includes an exposure section 10 for directing image light from a subject (not shown) toward an image sensor 12. Although not shown, the exposure section 10 includes conventional optics for directing the image light through a diaphragm, which regulates the optical aperture, and a shutter, which regulates exposure time. The sensor 12, which includes a two-dimensional array of photosites providing a predetermined picture resolution corresponding to the number of picture elements of the image, is a conventional charge-coupled device (CCD) using either well-known interline transfer or frame transfer techniques. Preferably, the sensor 12 is a high resolution device such as the model KAF-1400 sensor, a 1320(H)×1035(V)-element full-frame CCD imager manufactured by the Eastman Kodak Company. The sensor 12 is exposed to image light so that analog image charge information is generated in respective photosites. The charge information is applied to an output diode 14, which converts the charge information to analog image signals corresponding to respective picture elements. The analog image signals are applied to an A/D converter 16, which generates a digital image signal from the analog input signal for each picture element.

The digital signals are applied to an image buffer 18, which is a random access memory (RAM) with storage capacity for a plurality of still images. A control processor 20 generally controls the input section 2 of the camera by initiating and controlling exposure (by operation of the diaphragm and shutter (not shown) in the exposure section 10), by generating the horizontal and vertical clocks needed for driving the sensor 12, and for clocking image information therefrom, and by enabling the A/D converter 16 in conjunction with the image buffer 18 for each analog signal segment relating to a picture element. (The control Processor 20 would ordinarily include a microprocessor coupled with a system timing circuit.) Once a certain number of digital image signals have been accumulated in the image buffer 18, the stored signals are applied to a digital signal processor 22, which controls the compression and recording section of the camera. The processor 22 applies a compression algorithm to the digital image signals, and sends the compressed signals to a removable memory card 24 via a connector 26. A representative memory card is a 512 K-byte static random access memory (SRAM) available from Mitsubishi Corp. (A 1 megabyte memory card has been recently announced by ITT Canon.)

Since the compression and related processing ordinarily occurs over several steps, the intermediate products of the processing algorithm are stored in a processing buffer 28. (The processing buffer 28 may also be configured as part of the memory space of the image buffer 18.) The number of image signals needed in the image buffer 18 before digital processing can begin depends on the type of processing, that is, for a block transformation to begin, a block of signals including at least a portion of the image signals comprising a video frame must be available. Consequently, in most circumstances, the compression may commence as soon as the requisite block, e.g., of 16×16 picture elements, is present in the buffer 18.

The input section 2 operates at a rate commensurate with normal operation of the camera while compression, which consumes more time, can be relatively divorced from the input rate. The exposure section 10 exposes the sensor 12 to image light for a time period dependent upon exposure requirements, for example, a time period between 1/1,000 second and several seconds. The image charge is then swept from the photosites in the sensor 12, converted to a digital format, and written into the image buffer 18 during a standard rate, which may, for example, corresPond to a standard video field or frame rate. The repetition rate of the driving signals provided by the control processor 20 to the sensor 12, the A/D converter 16 and the buffer 18 are accordingly generated to achieve such a transfer. The processing throughput rate of the compression and recording section 4 is determined by the character of an image, i.e., the amount of detail versus redundant information, and the speed of the digital signal processor 22, and may take up to several seconds for an especially complex image. For this reason, the image buffer 18 shown in FIG. 1 provides for storage of a plurality of images, in effect allowing a series of images to "stack up" at video rates. Further description of the operation of the image buffer is provided in the aforementioned, copending U.S. patent application Ser. No. 349,566.

In addition to the full resolution, compressed image, the digital signal processor 22 generates a reduced resolution, or "thumbnail", image from the original image and outputs the reduced resolution image, together with the compressed image to the memory card 24 as a multi-format image file. A multi-format image file with a "thumbnail" area as it would appear on the memory card 24 is shown in FIG. 2A for one image and in FIG. 2B for several images. In each case, the reduced resolution image signals occupy a defined area near the beginning of each image file. A header may be used before each image file (FIG. 2A) or a directory can identify the location of each image file (FIG. 2B) on the card. On request from the processor 20, the digital signal processor 22 recovers the "thumbnail" image from the image file and outputs it on a line 22a to a display device 30.

Inasmuch as the "thumbnail" image is itself low resolution, the display device **30** may be a low resolution electro-optical device such as a liquid-crystal display. Alternatively, the display device **30** can be of higher resolution and display the "thumbnail" image in a window or portion of the display space.

The "thumbnail" image may be generated by any one of several methods. Average values could be determined for given areas of the original image, or the original image could be subsampled over its entire area. The resulting "thumbnail" data could be grey-scale or full color, and the number of bits/per pixel could vary to suit the needs of the application. In any case, the criteria would be that 1) the "thumbnail" data should add a minimum amount to the overall file size and 2) the "thumbnail" image should contain enough information to present a recognizable representation of the original image.

The digital signal processor **22** compresses each still video image stored in the image buffer **18** according to the image compression algorithm shown in FIG. **1B**. The compression algorithm begins with a discrete cosine transformation (block **33**) of each successive block of the image data to generate a corresponding block of cosine transform coefficients. It is well-known that compression techniques are greatly enhanced when applied to image data which has been previously transformed in accordance with a discrete cosine transform algorithm. The "thumbnail" image data is preferably taken from the discrete cosine transformation (as will be explained) and applied to a file controller (block **40**), which provides the "thumbnail" data on the line **22***a* to the display device **30** and combines the compressed data with the "thumbnail" data to provide the multi-format image file to the memory card **24**.

The cosine transform coefficients are rearranged in serial order by a block-to-serial conversion step (block **34**) described and illustrated in U.S. Pat. No. 4,772,956, "Dual Block Still Video Compander Processor," issued Sep. 20, 1988 to Roche et al, and which is assigned to the assignee of the present invention and incorporated by reference into the present patent application. The block-to-serial conversion step consists of arranging the discrete cosine transform coefficients in order of increasing spatial frequency, which corresponds to a zig-zag pattern illustrated in the Roche et al patent. The resulting serial string of transform coefficients is then subjected to conventional thresholding, normalization, and quantization (block **36**) and minimum redundancy encoding (block **38**). Thresholding discards data words of magnitudes less than a threshold number. Normalization entails dividing each data word by a divisor to yield a quotient. Quantization discards the fractional bits in the quotient. Minimum redundancy encoding is a technique well-known in the prior art for reducing the number of bits required to represent a frame of video information, without reduction in image quality, thereby greatly reducing the amount of storage that must be allocated to each still frame in the memory card **24**.

The compressed video data does not emerge from the processor **22** as a standard-length stream of bits, but as a variable number of bits dependent upon the complexity of the picture and the rules used for truncating bits. The memory space, therefore, allocated for each image in the memory card **24** can vary from image to image. The processor **22**, consequently, allocates memory space in the memory card **24** after each compression sequence for an image is completed so that the multi-format image files may be "packed" into the card as a continuum of compressed image data. This means the storage capacity, in terms of actual images, of the memory card is unknown in the beginning, and then gradually is specified as pictures are taken and the card is "filled". Alternatively, a fixed "maximum" space can be allocated in the memory card **24** for each multi-format image file; in this case, fewer images can be stored although the total capacity is always known.

What has been described to this point applies equally to monochrome or color pictures, except that color pictures require additional processing. For instance, if a multi-spectral color filter array (shown in broken line **39** in FIG. **1A**) overlies the image sensor **12**, the various colors are sorted out and processed differently for each color. This would be accomplished by an additional routine in the digital signal processor **22**. Such color filter array processing would precede the discrete cosine transform block **33** (FIG. **1B**) so that image compression can be done separately on each color and three compressed frames would be stored in the memory card **24** for each image.

Despite the degree of compression, a high quality digital image derived from a high resolution sensor can be large and, due to the necessity of decompression or expansion, require significant amounts of time to display due to size, resolution, and compression schemes. In keeping with the invention, the "thumbnail" or reduced resolution image is added to the compressed digital file format to make reviewing the image at any point in the imaging chain very fast. In terms of the multi-format file, a "thumbnail" image is a much smaller data file added to the original image data file. Although the image file may vary in length due to compression techniques, the "thumbnail" image would always be a known size based on the number of pixels in the original image.

An example would be a 1,280 by 1,024 pixel, 24-bit per pixel, compressed original image stored on a RAM-card mass storage device. This file might take on the order of 100 to 300 kilobytes of storage area depending on compression type. To display the image, it must first be expanded, and the resulting 4 Megabytes of information transferred to a display device. A "thumbnail" image is constructed by using the average value of each 16 by 16 pixel area in the original image to represent each pixel of the "thumbnail" image. If each pixel has an 8-bit grey scale, this would add about 5 Kilobytes to the overall image file size. To display the "thumbnail" image, no expansion is necessary, and only 5 Kilobytes of information needs to be transferred to the display device. The resulting image would be of sufficient quality to identify the subject matter of the original.

A "thumbnail" image generated from average values is preferable to one generated by simple subsampling (throwing away all but one pixel in a block). The averaged image looks more like the original with much less "blockiness" and less loss of detail. The preferred method for generating the "thumbnail" images uses the average or dc values from the DCT (Discrete Cosine Transform) algorithm, which were generated for compression of the image. The DCT algorithm produces one dc value for each block of the image being compressed. The dc value is a set of red, green, and blue values which are the mathematical average of the red, green and blue planes of pixels in the block. Alternatively, the mathematical average can be calculated outright over a block of pixels. This is done by actually

summing all the red values and dividing by the number of pixels to create an average red value, and then repeating for the green and blue planes.

A simplified block diagram is shown in FIG. 3A of a still video player for reproducing a picture or for making a hard copy print from the digital image signals stored in compressed format in the memory card **24**. With the card **24** inserted into a connector **100**, the digital signals are accessed and processed in the decoder **102**. The stored dc component of the transform (the "thumbnail" data) is directly applied to a selector **104** while the compressed image data is applied to an expander **106**. An expansion algorithm, which is the conventional inverse of the compression algorithm of FIG. 1B, is shown in FIG. 3B and implemented by the expander **106** which includes a conventional sequence of minimum redundancy decoding (block **106***a*), denormalization (block **106***b*), serial-to-block conversion (block **106***c*), and inverse discrete cosine transformation (block **106***d*). The digital image data is expanded block-by-block and stored in an image buffer **108** as a decompressed image. A conventional thermal printer **110** is connected to the buffer **108** for making a hard copy thermal print from the decompressed image. The output of the image buffer **108** is also connected to the selector **104**, which is under control of an operator-designated selection routine **112**. When a "thumbnail" image is to be observed, the selector **104** routes the "thumbnail" data through a digital-to-analog (D/A) converter **114** to a conventional CRT monitor **116**. Alternatively, the decompressed image signals are converted to analog form by the digital-to-analog (D/A) converter **114** and displayed on the conventional CRT monitor **116**.

A principal advantage of the file format shown in FIGS. 2A and 2B is that an image, with its associated "thumbnail" representation, can be easily separated from the collection of images on the memory card **24** and transmitted to external devices for further processing. For instance, the image file can be sent to the printer **110** and the "thumbnail" image can be quickly examined on the monitor **116** before committing to a print. Likewise, an image file can be easily downloaded to a transceiving device (not shown) and the "thumbnail" image can be examined before deciding to transmit. If the entire image file is transmitted, the "thumbnail" image can be quickly recovered at the receiving end for a preview of the final image. Moreover, for a plural number of images, the corresponding "thumbnail" images can be quickly accessed and displayed either in a mosaic frame or in sequence in order to select the desired full resolution image for printing, displaying, transmitting, etc. Furthermore, the "thumbnail" images can be played back by a dedicated player such as illustrated in FIG. 3A or by a personal computer or like device that is programmed to accomplish the functions outlined in FIG. 3A. In the latter case, the personal computer forms the interface between the memory card **24** and a printer, a monitor, a transceiver, etc.

The invention has been described in detail with particular reference to a presently preferred embodiment, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

What is claimed is:

1. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a digital memory, said imaging apparatus including an image sensor having an array of photosites corresponding to picture elements of the still image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to a predetermined picture resolution;

means for subsampling said digital image signals to generate reduced resolution image signals corresponding to a picture resolution lower than said predetermined resolution;

means for generating a multi-format image file representative of plural resolutions of the still image from the combination of said digital image signals and said reduced resolution image signals, said combination forming a singular file structure in which said reduced resolution image signals occupy a defined file area in relation to said digital image signals and are commonly accessible therewith for display and processing; and

means for storing the image file in said digital memory.

2. The apparatus as claimed in claim **1** further including:

display means for generating a display image;

means for selecting an image file stored in said digital memory; and

means for applying said reduced resolution image signals from said stored image file to said display means to generate a low resolution display of the still image.

3. The apparatus as claimed in claim **1** in which the sensor is sequentially exposed to a plurality of still images, said digital image signals and said reduced resolution image signals therefore corresponding to said plurality of images, said file generating means generating a separate multi-format image file for each still image from the digital image signals and the reduced resolution signals corresponding thereto, and said storing means storing each multi-format image file in said digital memory.

4. Electronic still imaging apparatus employing digital processing of image signals acquired from a plurality of still images and storage of the processed image signals in a removable digital memory, said imaging apparatus including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of an image and means for exposing said sensor to image light so that analog image information is generated in respective photosites for each acquired image, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to respective picture elements;

an image buffer for storing digital image signals corresponding to blocks of picture elements;

digital processing means for transforming blocks of stored digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a stream of compressed signals;

means responsive to said stored digital image signals for generating reduced resolution image signals corresponding to a reduced resolution version of each image;

means for forming a multi-format image file representative of plural versions of each acquired image,

each image file including the reduced resolution image signals and the compressed signals for a particular still image; and

means for downloading said image file for each acquired image to said removable digital memory.

5. The apparatus as claimed in claim 4 in which the reduced resolution image signals are generated from an average value of the digital image signals corresponding to each block of picture elements.

6. The apparatus as claimed in claim 5 in which the average values of the digital image signals are derived from the transform coefficient signals.

7. Electronic image processing apparatus employing digital processing of image signals corresponding to picture elements of a still image and storage of the processed image signals in a digital memory, said image processing apparatus comprising:

an image buffer for storing digital image signals corresponding to blocks of picture elements;

digital processing means for transforming blocks of stored digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a stream of compressed image signals, said digital processing means further generating reduced resolution image signals from said stored digital image signals;

means for generating a multi-format image file representative of plural resolutions of the still image, said image file including the reduced resolution image signals and the compressed image signals; and

means responsive to said digital processing means for downloading the image file to said digital memory.

8. Apparatus as claimed in claim 7 in which said digital processing means generates an average signal for each block of stored digital image signals and said reduced resolution image signals are formed from said average signals.

9. An electronic image processing system employing digital processing of image signals corresponding to picture elements of a still image and storage of the processed image signals in a digital memory, said image processing system comprising:

an image buffer for storing digital image signals corresponding to blocks of picture elements;

digital processing means for transforming blocks of stored digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a stream of compressed image signals, said digital processing means further generating reduced resolution image signals from said stored digital image signals;

means for generating a multi-format image file representative of plural resolutions of the still image, said image file including the reduced resolution image signals and the compressed image signals;

means responsive to said digital processing means for downloading the image file to said digital memory;

means for selecting an image file stored in said digital memory; and

playback means for operating on the selected image file and generating a reduced resolution image display from said reduced resolution image signals.

10. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a digital memory, said imaging apparatus including an image sensor having an array of photosites corresponding to picture elements of the still image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to a predetermined picture resolution;

means for averaging said digital image signals over local areas of the still image to generate reduced resolution image signals corresponding to a picture resolution lower than said predetermined resolution;

means for generating a multi-format image file representative of plural resolutions of the still image from the combination of said digital image signals and said reduced resolution image signals, said combination forming a singular file structure in which said reduced resolution image signals occupy a defined file area in relation to said digital image signals and are commonly accessible therewith for display and processing; and

means for storing the image file in said digital memory.

11. The apparatus as claimed in claim 10 further including:

display means for generating a display image;

means for selecting an image file stored in said digital memory; and

means for applying said reduced resolution image signals from said stored image file to said display means to generate a low resolution display of the still image.

12. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a digital memory, said imaging apparatus including an image sensor having an array of photosites corresponding to picture elements of the still image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to a predetermined picture resolution;

means operating on blocks of digital image signals for compressing said digital image signals and generating averages over said blocks;

means responsive to said averages produced by said compressing means for generating reduced resolution image signals corresponding to a picture resolution lower than said predetermined resolution;

means for generating a multi-format image file representative of plural resolutions of the still image from the combination of said compressed digital image signals and said reduced resolution image signals, said combination forming a singular file structure in which said reduced resolution image signals occupy a defined file area in relation to said compressed digital image signals and are commonly accessible therewith for display and processing; and

means for storing the image file in said digital memory.

13. The apparatus as claimed in claim 12 in which said compressing means compresses the digital image signals in a plurality of stages, one stage including the performance of a discrete cosine transform on blocks of digital

image signals and another stage including minimum redundancy encoding of the transformed image signals.

14. The apparatus as claimed in claim **13** wherein said discrete cosine transform produces a dc component and said reduced resolution image signals are generated from the dc component of the discrete cosine transform.

15. The apparatus as claimed in claim **12** further including:

display means for generating a display image;

means for selecting an image file stored in said digital memory; and

means for applying said reduced resolution image signals from said stored image file to said display means to generate a low resolution display of the still image.

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EXHIBIT 50

SEALED DOCUMENT